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Surface Effects of Radiation on Semiconductor Devices*

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A brief review of surface physics is given as background for the subsequent discussion on the role of surfaces in the behavior of semiconductor devices. The effects of channels and surface generation-recombination on p-n junctions and transistor characteristics are discussed.

The observed effects of ionizing radiation on nonpassivated, gas-filled transistors are interpreted in terms of a model in which ions formed in the gas ambient deposit charge on the device surface. The resultant surface charge buildup creates channels on the device surface which cause a decrease in h_{FE} and increase in I_{CBO} . Saturation, recovery, and the effects of dose rate and bias are also discussed.

Degradation of planar passivated transistors and other devices employing SiO_2 layers due to radiation is similar to that observed for nonpassivated devices. Surface charge buildup affects the device surface and leads to degradation. The bulk of experimental evidence points to accumulation of positive charge at the SiO_2–Si interface as the cause of degradation. Several possible means of charge buildup at the interface are discussed. However, the process responsible has not, as yet, been identified.

The direction of future experiments is discussed, particularly of those experiments which may yield information about the part played by radiation in positive charge accumulation at the SiO_2–Si interface.

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I. INTRODUCTION

When a semiconductor is exposed to nuclear radiation, two basically different effects may occur. First, the radiation will cause ionization through one of a number of electronic excitation processes. Second, if the radiation energy exceeds a threshold value which depends on the nature of the irradiating particle, some of the atoms in the semiconductor lattice will be displaced. If the semiconductor exposed to radiation is part of a device, the device characteristics will change; the changes depend on such factors as the nature and energy of the radiation, the materials and geometry of the device, and even the processes used in manufacturing the device. The changes in characteristics which occur when these effects take place in the bulk of a device have been investigated for some time and are quite well understood in terms of the usual physics of solids. However, effects can also occur at the surface of a device, giving rise to the so-called surface effects which have only more recently received attention and which are governed by the less well understood physics of surfaces.

The failure of the *Telstar*® satellite in 1962 was explained in terms of surface damage to transistors in the command circuits, damage caused by radiation received during transit through the Van Allen belt.[1] From the experience gained in analyzing this failure, it is apparent that surface effects of radiation may often control the behavior of solid state devices subjected to nuclear radiation. In present-day semiconductor technology, the effects of radiation damage in the bulk have been reduced in transistors by using very shallow, diffused junctions. As a result, the surfaces have become the most radiation sensitive areas of these devices. Thus, a knowledge of surface effects is necessary if the decrease in sensitivity to bulk radiation effects is to be fully exploited.

The purpose of this paper is to present as unified and comprehensive a picture as possible of the work done to date on the surface effects of radiation on semiconductor devices. The task is hampered somewhat by the way in which much of the information on radiation effects is presented in the literature. Many authors do not distinguish between bulk and surface effects, and indeed in many experiments it is virtually impossible to do so. For this reason this paper will be, for the most part, restricted to those experiments which deal specifically with surface effects.

Some areas of the surface problem appear to be fairly well understood. The degradation process in nonpassivated devices in gaseous ambients has been satisfactorily explained in terms of surface channeling at exposed p-n junction surfaces. On the other hand, no such satisfactory

picture has been published for planar transistors. The results at the moment are somewhat confused, contradictory, and incomplete. It is hoped that this summary may help to illuminate the problem and suggest paths for future studies.

A brief discussion of the present physical theory of surfaces, as required for an understanding of device degradation, will be given before starting a discussion of experimental results and specific models for radiation effects on surfaces since it is against this background that radiation effects must be explained. For a more complete discussion of surfaces, the reader is referred to works by Many, Goldstein and Grover,[2] Watkins,[3] and Law.[4]

II. SURFACE PHYSICS

2.1 *Surface Charges and Surface Potential*

An atomically clean crystal surface, such as might be found upon cleaving a crystal, would show broken or dangling bonds associated with the surface atoms. If the bonds are covalent, then presumably each bond, which could hold two electrons, would be half-filled and, therefore, is able to act as an acceptor state. If these acceptor states become filled, the crystal surface would then have a net negative charge. One might, therefore, expect to find a negative surface charge of $\approx 10^{15}$ electrons per cm^2, i.e., one excess electron per surface atom. If the crystal is a metal, the surface charge would be neutralized in a depth of a few angstrom units since metals have a high density of charge carriers. For a semiconductor, however, the much smaller concentration of charge carriers means that the effects of the surface charge will be present as far as $\approx 1\mu$ into the crystal. It should be noted that in this surface region the charge carriers will be holes regardless of the conductivity type of the bulk; i.e., the surface will always be p-type.

Such atomically clean surfaces have been achieved on both silicon and germanium, but they can only be maintained in a very clean vacuum. In any other ambient, the highly reactive surfaces of these semiconductors will readily absorb several atomic layers from the ambient. These layers (usually oxide) will neutralize most of the surface states due to broken bonds. Some energy states will still exist at the crystal surface, however, either as a result of unsaturated lattice bonds or as a result of impurities or imperfections at the semiconductor surface. The density of these states is typically 10^{11} to 10^{12} per cm^2. These states, called "fast" states, are in good electrical contact with the bulk material and have relaxation times of about 10^{-7} s. As a consequence, the fast surface

states are often the controlling centers of minority carrier recombination and generation.

In addition to the states at the interface, states arise which are caused by ions in or on the surface of the film adsorbed on a semiconductor. These states may be sources or sinks for mobile carriers. Because of poor electrical contact between these states and the semiconductor, mobile carriers are exchanged slowly between the two, presumably by some tunneling or diffusion process. These ionic states are called the "slow" surface states and have relaxation times from 10^{-3} seconds up to many minutes. Since the states may be positively or negatively charged, they can give rise to surface layers of either p- or n-type. Although little quantitative information is available, it is believed that the densities of slow states are of the order of 10^{12} to 10^{13} per cm^2.

For Si surfaces covered by a thick layer ($\approx 10^3$–10^4 Å) of deliberately grown oxide, so-called passivated surfaces, the situation is more complicated and the distinction between fast and slow surface states is not a very meaningful one. Surface charges may arise in these thick oxides for several different reasons and may be located on either surface of the oxide or anywhere within the oxide itself. It is customary, therefore, to discuss effects on passivated Si surfaces in terms of surface charge in the oxide and states at the SiO_2–Si interface. These interface states are essentially fast states similar to those discussed above for nonpassivated surfaces.

Charges on a semiconductor surface trapped in either slow or fast states will attract or repel mobile charge carriers in the bulk region near the surface so as to neutralized the surface charge and shield the interior from their effects. The net result is a bending of the energy bands of the material in the surface region. The amount of bending of the bands is usually specified quantitatively by the surface potential, U_s. As shown in Fig. 1, U_s is the difference between the Fermi level, E_F, and the intrinsic Fermi level, E_i, at the surface.

$$U_s = (E_F - E_i)_{x=0} .$$

Depending on the amount and direction of bending of the bands, one of three types of surface region will arise:

(*i*) A depletion region is formed if the mobile carrier concentration is much less than the concentration of ionized impurities. For an n-type material this will occur if the bands bend up ($U_s < 0$) at the surface, making states for the electrons near the surface energetically less accessible. For a p-type material the bands must bend down to form a depletion region ($U_s > 0$).

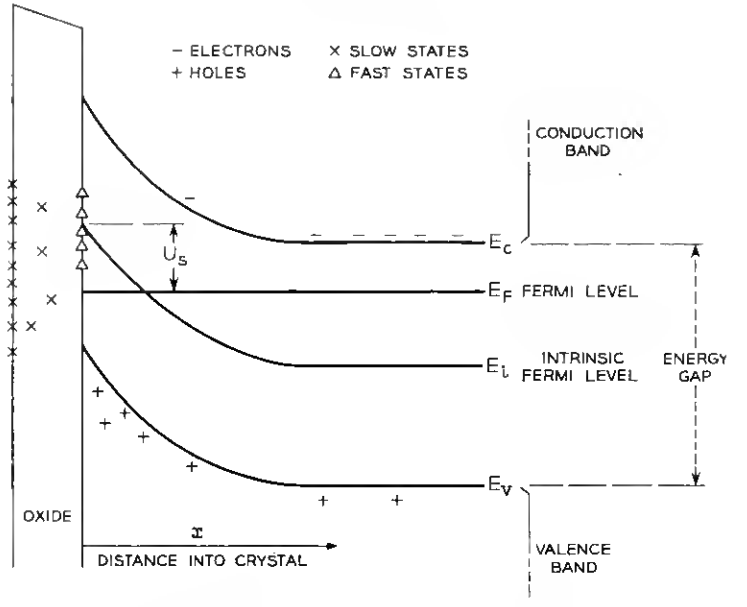

Fig. 1 — Band structure at the surface of a semiconductor.

(*ii*) A depletion layer may become an inversion layer if the bending of the bands is increased sufficiently. This case is illustrated in Fig. 1 for an n-type material where the minority carriers dominate in the surface region. An inversion layer will, of course, have a depletion region behind it.

(*iii*) If for any reason the bands bend down for an n-type (or up for a p-type) semiconductor, excess majority carriers will collect in the surface region and an accumulation layer will result. The three cases are illustrated for both n- and p-type materials in Fig. 2.

It is apparent from the above discussion that the concentration of charge carriers and hence the conductivity of the surface layer of a semiconductor may differ considerably from the bulk values. In practice it is possible to obtain valuable information about surface effects by purposely changing the surface potential (and hence the bending of the bands) of a semiconductor and observing the resultant changes in surface conductivity.

2.2 *Control of Surface Potential*

The surface potential of a semiconductor is controlled through the charge in the surface states. In this regard the slow states are the more

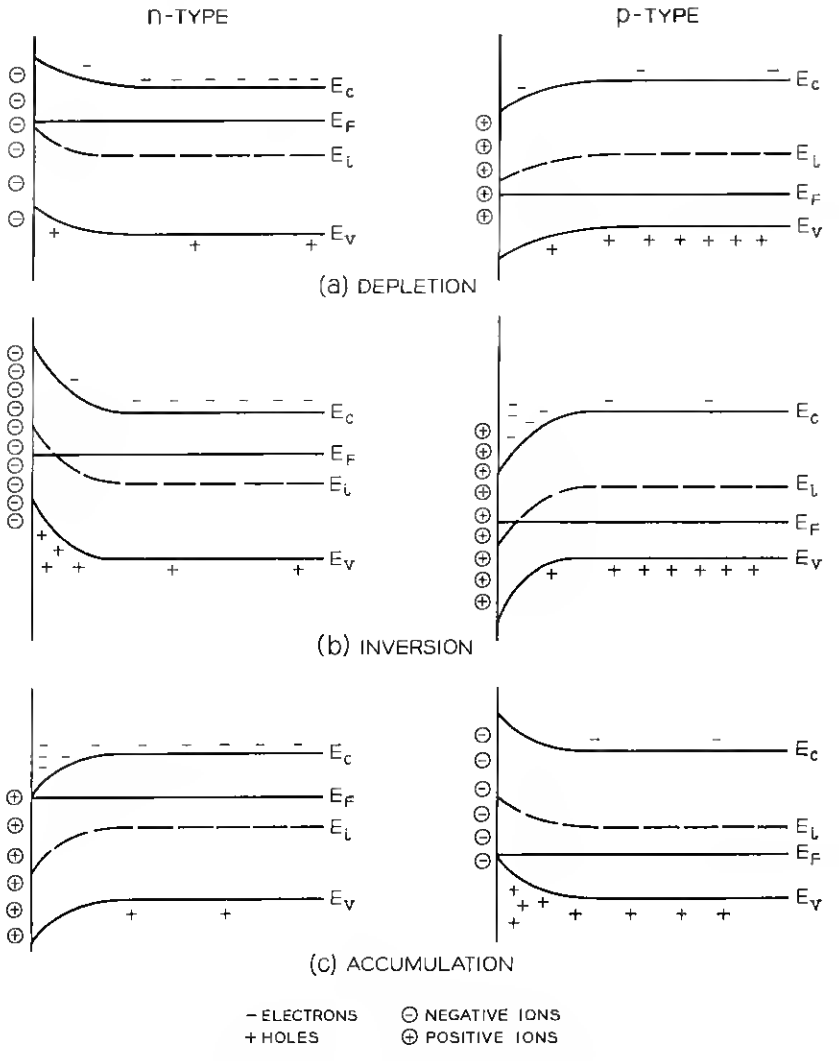

Fig. 2 — Depletion, inversion, and accumulation surface layers for n- and p-type semiconductors.

important since they are usually at least an order of magnitude more numerous than the fast states. There are two methods commonly used for controlling surface charge. In one method the charge is determined by the choice of ambient. For example, gaseous ambients such as oxygen or ozone have strong electron affinities and induce a negative charge

on the surface which attracts to it mobile holes. Water vapor and ammonia, on the other hand, produce a positive surface charge, i.e., contribute donor states. Thus, by exposing a semiconductor to the appropriate ambient it is possible to produce, within reasonable limits, a desired surface potential.

The thermally grown SiO_2 layer on Si devices is a particular type of ambient widely used in device fabrication. This oxide stabilizes the surface by saturating the dangling bonds of the Si surface and by separating the Si from the slow states by the thickness of the oxide. This so-called passivation technique, although it does not completely isolate the semiconductor from the ambient, does reduce its sensitivity to ambient variations.

A second method of controlling surface potential is through the use of a field plate. As shown in Fig. 3, a metal field plate is placed parallel to the semiconductor surface so as to form a capacitor between it and the semiconductor. The space between the field plate and the semiconductor is filled with some insulator such as SiO_2. The conductivity type of the semiconductor surface layer may be controlled by the applied potential. For example, if the field plate is positive with respect to the semiconductor, electrons will be attracted to and holes repelled from the surface, with the result that the surface layer tends to become more n-type. By the same argument, if the polarity of the potential is reversed, a tendency toward a p-type surface results. The field effect method of controlling surface conductivity is the operating principle of the metal-oxide-semiconductor field effect transistor (MOS-FET). In this device the conductivity of the base, and hence the source-to-drain current, is controlled by the gate (field plate) potential.

2.3 *Surface Recombination Velocity*

The fast states at a semiconductor surface are very important from a device standpoint since they act as recombination centers. These

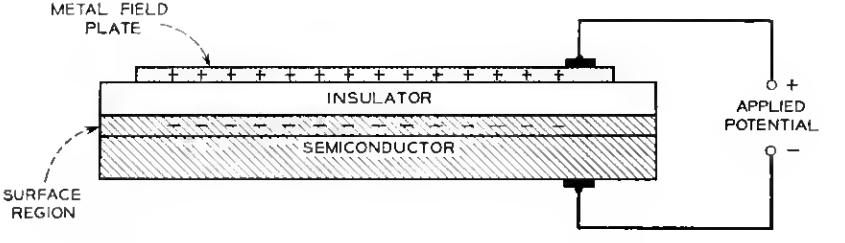

Fig. 3—Field plate method of controlling surface potential.

centers are relatively more important than bulk recombination centers since they have large capture cross sections and are present with an effectively higher density. As a consequence, within a few diffusion lengths of the surface, generation and recombination are controlled by the fast surface states. The activity of the surface states is measured by the surface recombination velocity, S. The particle current, J/q, of hole-electron pairs combining at the surface per cm^2 per s is proportional to the excess minority carrier density at the surface, Δn; i.e.,

$$J/q = S\Delta n$$

which defines S as the constant of proportionality. S has the dimensions of velocity. It is to be expected that S will change with variations in U_s, i.e., with variations in the surface charge. For S to be near maximum, the densities of holes and electrons at the surface should be approximately equal (assuming equal capture cross sections for the two carriers). This condition is fulfilled when $E_F = E_i$. As U_s changes

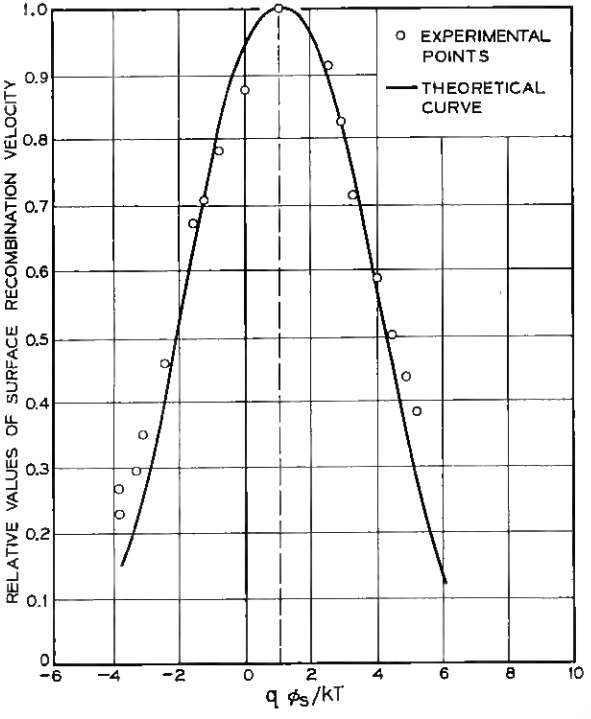

Fig. 4—Variation of surface recombination velocity with surface potential (after Many and Gerlich, Ref. 5).

in either direction from zero, the bands bend up or down causing the concentration of one type of carrier to increase and the other to decrease. The result in either case is a decrease in S. Fig. 4 shows, as an illustration, the variation of S with surface potential, ϕ_s, for a Ge surface as reported by Many and Gerlich.[5] It is apparent that changes in S of almost an order of magnitude are possible. The recombination velocity for Si surfaces has been found to be larger than that for Ge, but shows a similar dependence on U_s.[6]

2.4 *Channeling*

An important result of surface states which are sufficiently dense to produce an inversion layer at the surface is the effect known as channeling. Brown[7] discovered that the anomalous leakage current between the n-regions of an npn structure was the result of channels, i.e., inversion layers, formed across the p-region, which provided a conduction path of the same conductivity type as the end regions. Channel formation may occur at any p-n junction, generally on the low conductivity side of the junction. Channels have the effect of adding currents in parallel with the main junction currents. The times involved in channel formation indicate that the phenomenon is connected with the slow surface states. It will become apparent that channeling is the dominant surface effect for many semiconductor devices.

III. EFFECTS OF SURFACES ON DEVICES

3.1 *p-n Junction Forward Characteristics*

The effect of surface recombination and channel formation on p-n junction forward characteristics has been discussed by Sah.[8] The junction current can be divided into several components based on the location of the carrier recombination-generation. The components are (see Fig. 5):

(*i*) bulk recombination-generation on either side of the junction,
(*ii*) transition region bulk recombination-generation current,
(*iii*) surface recombination-generation current on either side of the junction,
(*iv*) transition region surface recombination-generation current, and
(*v*) surface channel current.

The first component is the usual diffusion current of a forward-biased junction. The second component arises from electron-hole generation by traps located in the bulk of the transition region. These two components are not affected by surface conditions. Component (*iii*) is the diffusion

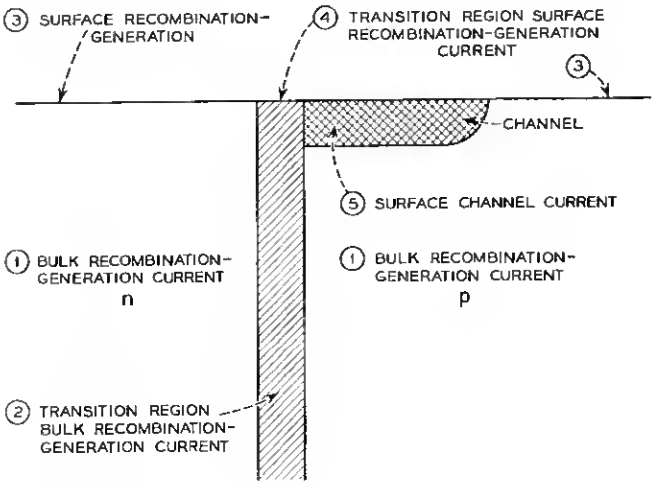

Fig. 5—Locations of carrier recombination-generation at a forward-biased p-n junction.

current of the junction arising from surface generation-recombination (Sah includes this component as part of component (*i*)). Component (*iv*) is the result of surface generation of minority carriers at the surface of the transition region. The surface current represented by component (*v*) is caused by generation in channel regions, if present, and the adjacent bulk material.

The voltage dependence of the five components may each be described by an equation of the form

$$I = I_s \exp (qV/mkT)$$

for a junction voltage, $V > 4kT/q$. $m \approx 1$ for components (*i*) and (*iii*), $1 < m < 2$ for components (*ii*) and (*iv*), and $2 < m < 4$ component (*v*).

For components (*iii*), (*iv*), and (*v*), m and I_s in the expression for I are functions of the surface potential; hence, the diode forward characteristics depend, through this potential, on the surface charge. When channels are present at a junction, component (*v*) will usually dominate over components (*iii*) and (*iv*) and the surface part of the forward diode current will be determined by the channel values for m and I_s.

3.2 *p-n Junction Reverse Characteristics*

3.2.1 *Leakage Current*

The reverse leakage current of a p-n junction is also the sum of several components resulting from the inverse of the processes described above

for tbe forward current. Thus, a bulk component arises from thermally generated minority carriers which are created within or diffuse to tbe spaee cbarge region and are swept across the junction by the reverse bias field. The surface near the junction is also a souree of minority carriers and produces components of reverse current from the surface both outside and inside and junction space charge region.

If channeling is present when a diode is under reverse bias, the reverse current will be increased for two reasons. First, the channel increases the effective area of the junction and thereby increases the number of thermally generated minority carriers diffusing across the junction. Second, an increase in arca takes place at the surface which, because of surface sites, has a high generation of carriers. A further result of the increased junction area is an increased junction capacity (which provides a eonvenient means of detecting the presence of ehannels).

The above explanation appears to be satisfactory to explain the reverse current observed in most Si and Ge junctions. However, for some Si junetions, particularly of the p^+n type, the reverse leakage currents is often too large to be explained as entirely the result of generation-recombination in the increasd junction area at the surface. Grove and Fitzgerald[9] have explained the anomalous current as the result of breakdown through the narrow depletion layer of the induced p-n junction caused by the channel.

3.2.2 *Breakdown*

The breakdown voltage of a reverse-biased junction is, in many cases, reduced below the valuc expected for bulk breakdown by surface conditions at the junction. Surface breakdown, like bulk breakdown, is an avalanche process and takes place at localized areas of the surface. It has been found that an inversion layer formed on the high resistivity side of a junction raises thc breakdown voltage, while formation of an accumulation layer tends to lower it.

3.2.3 $1/f$ *Noise*

Semiconductor devices often exhibit a noise whose spectral output is inversely proportional to frequency and which is referred to as $1/f$ noise. It is believed that this noise originates at the semiconductor surface; certainly it is very sensitive to surface conditions. According to McWhorter,[10] $1/f$ noise is the result of fluctuations in the eharge in tbe slow states which cause corresponding changes in the semiconduetor conductivity. Experimentally, it is known that $1/f$ noise increases when the semiconductor surface layer changes from accumulation to inver-

sion. Atalla and his associates[11] have found that SiO_2 passivation significantly reduces $1/f$ noise.

3.3 *Effects of Surface Recombination and Channeling on Junction Transistors*

The effects of channeling and surface recombination on transistors are somewhat more complicated than for simple p-n junctions. As might be expected, I_{CBO} for the transistor behaves in a similar way to a diode-junction reverse current. I_{CBO} may also be increased by the formation of a channel across the base region so as to provide a leakage path from emitter to collector.

The current gain of a transistor may be affected by both channel and surface recombination in the region of the emitter-base junction. The common emitter gain, $h_{FE} = (I_C - I_{CEO})/I_B$ is influenced through I_B. If the base transport factor (β) of a transistor is decreased because of increased surface recombination at the base surface, then I_B is increased to supply majority carriers for recombination. This recombination corresponds to an increase in a component of the emitter current with an exp (qV/mkT) dependence where $m \approx 1$. Generation-recombination at the surface of the emitter-base transition region lowers the emitter efficiency (γ) and also decreases h_{FE}. This corresponds to an increase in an emitter current component with an exp (qV/mkT) dependence with $1 < m < 2$. These effects of surface recombination and channeling on junction transistor characteristics have received experimental support from the work on Sah,[8] Kuper,[12] and Iwersen et al.[13] Kuper found that the base current, I_B, of diffused base Ge transistors was quite sensitive to surface traps at the surface of the emitter-space charge region. The effect of these traps on recombination could be increased by removing water from the surface oxide, resulting in an order of magnitude decrease in h_{FE}. The surface region of the emitter-base junction would thus appear to be the region which controls the common emitter current gain in Ge transistors.

The gain degradation in Si transistors at low currents was investigated by Iwersen. Fig. 6 shows a typical dependence obtained by Iwersen of I_C and I_B on V_{EB} for silicon npn transistors. The I_B characteristic has two components, an "ideal" one at high currents with $I_B \propto \exp(qV_{EB}/kT)$ and a "nonideal" one at low currents with $I_B \propto \exp(qV_{EB}/mkT)$ with $m \approx 2$. The latter component according to Sah's model could come from recombination in the emitter-base space charge region either in the bulk or at the surface. Iwersen et al used transistor-like structures with an additional electrode connected

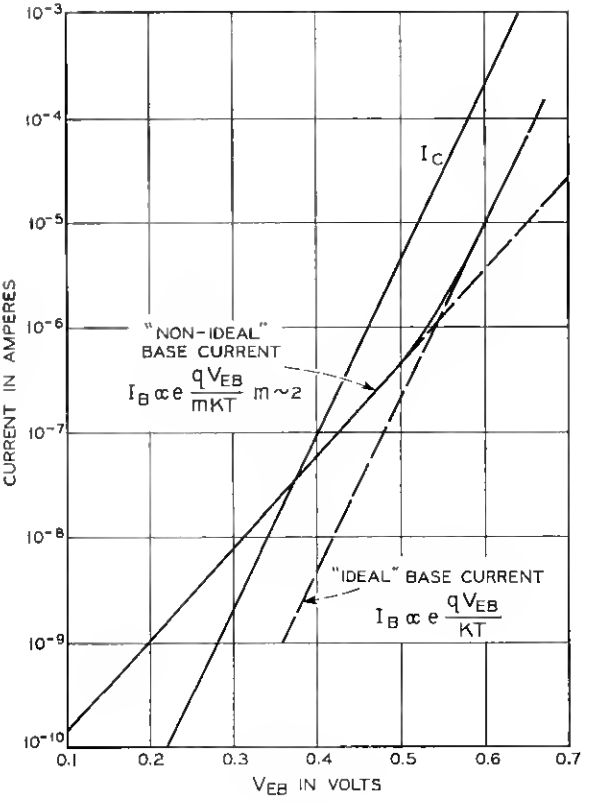

Fig. 6—Typical I_C , I_B vs V_{EB} curves for Si npn transistors (after Iwersen et al, Ref. 13).

to the emitter with which they could shift the forward-biased part of the emitter away from the surface. Under these conditions the I_B characteristic showed the "ideal" behavior illustrated in Fig. 6. Thus, the decrease in h_{FE} at low currents appears to arise from recombination at the surface of the emitter-base space charge region. This technique for separating surface and bulk components is a very useful one and is currently being exploited to separate bulk and surface effects after irradiation as well.

Neither Kuper nor Iwersen et al discuss the effect of channels at the emitter-base junction. Sah, however, has investigated the effects of channels through the use of a special planar transistor which had a metal gate over the surface region of the emitter-base junction. A channel could be induced on the base surface by a suitable selection of

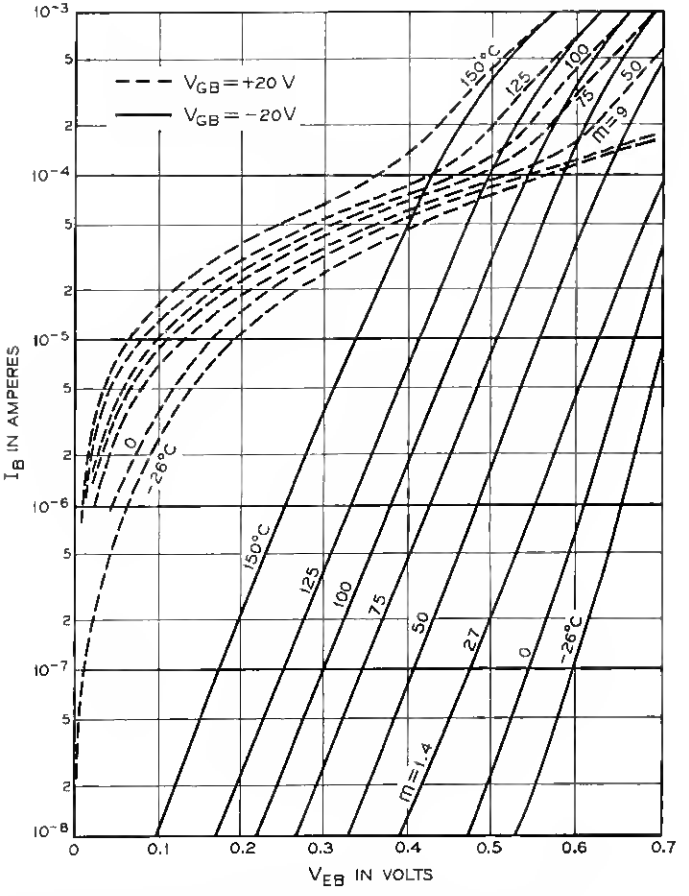

Fig. 7—Forward emitter characteristics for a surface channel (V_{GB} = +20V) and for no surface channel (V_{GB} = −20V) (after Sah, Ref. 8).

gate potential, V_{GB}. Fig. 7 shows the junction current, I_B, as a function of junction voltage, V_{EB}, for temperatures ranging from −26° to 150°C. The solid curves correspond to the absence of channels (V_{GB} = −20V) while the dashed curves are for the case of channels present (V_{GB} = +20V). It is apparent from Fig. 7 that m is much larger ($m \approx 9$ for channels as compared with $m \approx 1.4$ for no channels) when channels are present and that when channels are present the channel components of the junction current will dominate. It is apparent that I_B is much less temperature dependent when channels are present.

According to Sah, the surface recombination current is considerably

higher on a bare surface than on an oxide-protected surface. Hence, we should expect to find a higher h_{FE} for protected devices. As predicted, Sah finds the gains for Si planar transistors are higher at all collector currents for oxide-protected devices than for the same devices after the oxide has been removed.

IV. SURFACE EFFECTS OF RADIATION ON NONPASSIVATED MATERIALS AND DEVICES

4.1 *Introduction*

There are two types of effects on the bulk of a semiconductor resulting from irradiation by energetic particles or photons. First, new defects are created which introduce additional energy levels in the energy gap of the semiconductor. Second, intense ionization is produced, most of which decays quickly, but a certain fraction of which may be trapped in rather long-lived excited states. The kind and number of defect states introduced into the bulk are very sensitive to the nature of the bombarding particle and its energy. On the other hand, the ionization produced in the bulk is presumably sensitive only to the total energy adsorbed.

The surface of a semiconductor is presumed to be a highly imperfect structure. Hence, it has been tacitly assumed that the radiation levels which significantly affect the number of bulk defect states could not similarly affect the number of surface defect states. This assumption may be invalid for the reasons discussed in the following paragraphs.

It is believed that the primary defects introduced by radiation are vacancies and interstitials. However, there is strong experimental evidence that these primary defects interact almost immediately with existing crystal defects. If they do not do so, there appears to be a strong likelihood that the vacancies and interstitials annihilate one another, i.e., that frozen-in vacancies and interstitials per se do not exist. There is also strong experimental evidence indicating that existing defects in the semiconductor crystal may often be electrically inactive but become electrically active when attached to a primary radiation defect. Hence, the surface, with its high concentration of existing defects, may be a sink for primary radiation defects. The result of such an interaction could be a significant change in the number of impurity levels at the surface upon irradiation, i.e., an increase in the density of fast states at the interface of the semiconductor and any adsorbed surface layer. In addition, the density of active (charged) slow states can be increased by purely electronic processes produced by ionizing

radiation effects within or on the adsorbed surface layer. These changes in charge state of the surface defects can be very long-lived because of the weak electronic interaction of these surface defects and the bulk of the semiconductor.

The evidence on nonpassivated devices tends to support the picture that the predominant effects of radiation on nonpassivated surfaces are changes in the charge in slow states rather than the creation of new defects. Hence, most experiments on surface effects have not concerned themselves with the nature of the ionizing particle but only with the energy absorbed (dose) at the surface. Most experiments have, therefore, been done with Co^{60} gamma rays as a matter of convenience, with a few investigations using energetic electrons. (The calculation of absorbed dose for an electron beam is discussed in Appendix B.) The possibility outlined above for the creation of additional defect states by the interaction of primary defects with existing defects and their dependence on the nature of the bombarding particle has not been adequately explored.

4.2 *Effects of Radiation on Semiconductor Surfaces*

There have been limited experimental studies on single crystal semiconductor samples of the effects of ionizing radiation on surface phenomena. Among the studies that could be cited is the work of Spear,[14,15] who investigated the effects of radiation on the photoconductive response in germanium down to energies of 0.5 eV, i.e., well below the absorption band edge. This response arises from deep-lying surface states. Irradiation with very low energy electrons ($\approx$5 keV) was found to quench this photoconductivity. Spear attributed this quenching to radiation-induced changes in the surface potential with the result that the surface became more n-type. Similar changes in surface potential of n-type Si were found by Spear for both 3 and 500 keV electron irradiation.

The effects of irradiation by Co^{60} gamma rays and energetic electrons on the surface recombination velocity in n-type Ge have been studied by Komatsubara.[16,17] He used alloyed p-n junctions with a nickel field plate on the opposite side of the Ge wafer from the alloyed junction. By using a wafer whose thickness was small compared to a diffusion length, he made the reverse current of the junction, I_s, proportional to the surface recombination velocity, S. In this way he was able to obtain directly an oscilloscope presentation of the variation of recombination velocity with surface potential, U_s, using a 50-Hz ac voltage on the field plate. His results before and after various levels of γ bombardment are shown in Fig. 8 and can be compared with the theoretical

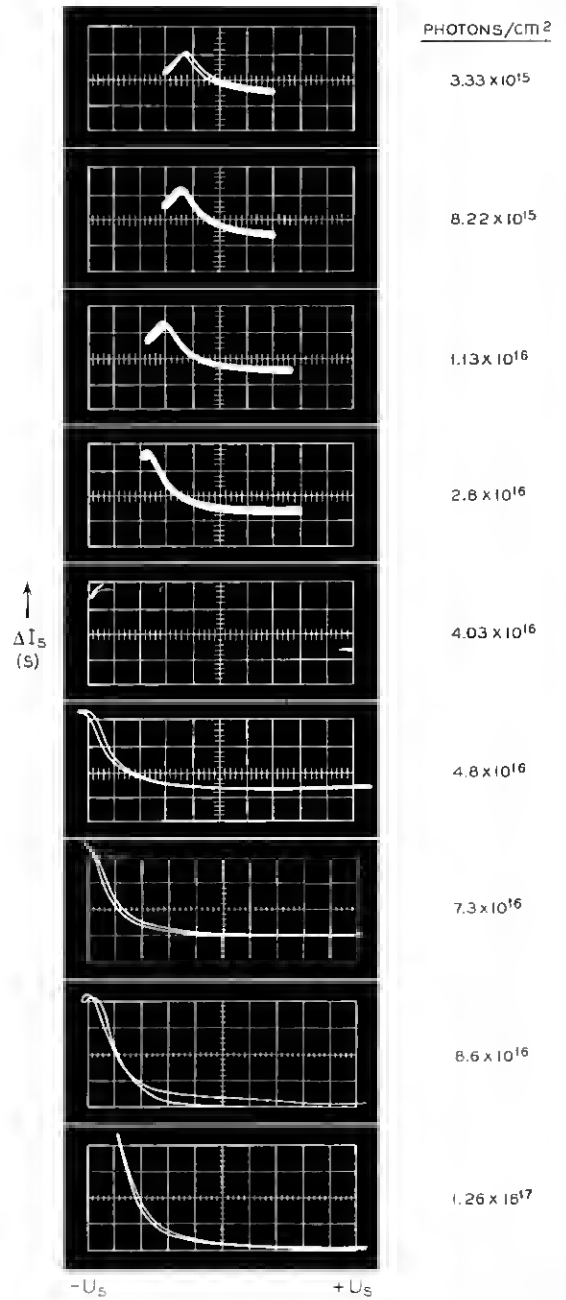

Fig. 8 — Change of I_s vs U_s curves of 30 ohm-cm n-type Ge with radiation (after Komatsubara, Ref. 17).

variation shown in Fig. 4. There is obviously a considerable shift in the surface potential, which Komatsubara attributed to new fast surface states produced by the radiation.

4.3 *Effects of Ion Bombardment on P-Type Silicon Surfaces*

Considerable experimental evidence (to be reviewed later) has established that many of the radiation effects on semiconductor devices can be traced to the ionization of the ambient by the radiation with subsequent migration of the ions to the semiconductor surface and resultant changes in the density of *slow* surface states.

In an attempt to discover more about the processes involved at the surface of an irradiated semiconductor device, Estrup[18] investigated the effects of ion bombardment on the surface conductivity of p-type Si. To do this he placed a slab of the material, into which n+ regions had been diffused at either end, in a gaseous discharge. By a suitable selection of electrode potentials and gases he was able to bombard the Si surface with either electrons or positive ions. By measuring the current between the n+ regions, Estrup determined whether n-type channels had been formed.

When the material was exposed to positive ions, a large increase in the current, I, through the sample was observed, indicating the formation of a highly conducting channel. Fig. 9 shows the increase in current, ΔI, as a function of the total ion charge, Q, impinging on the surface for two ion currents, J_a and $J_b (J_a > J_b)$. Initially the rate of increase of I is very large, but it gradually diminishes until eventually I levels off, i.e., the surface effect saturates. The buildup of surface charge was

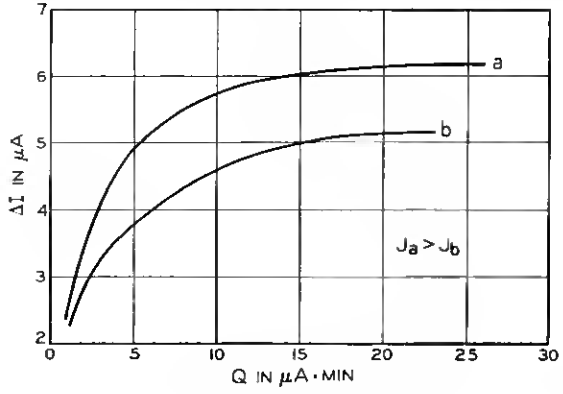

Fig. 9 — Current increase vs total ion charge reaching the Si surface (after Estrup, Ref. 18).

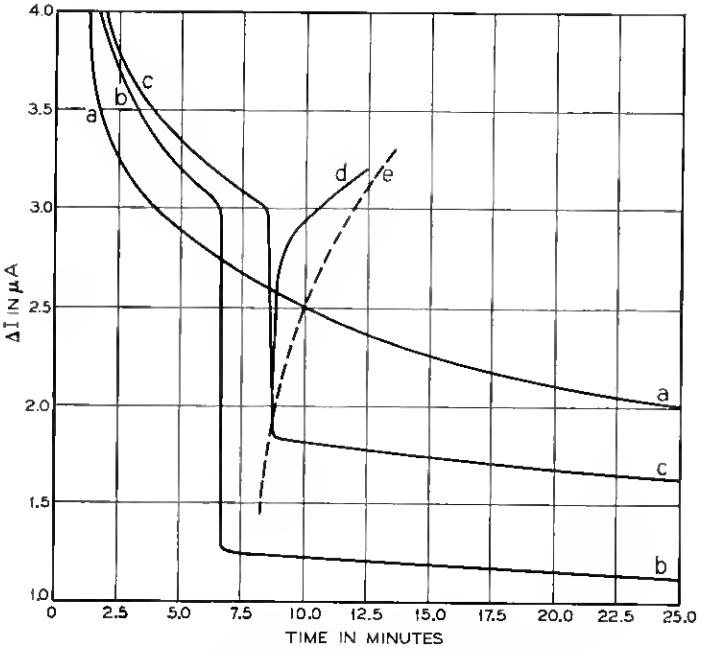

Fig. 10—Current increase as a function of time (after Estrup, Ref. 18).

found to depend primarily on the ion current, the bulk material conductivity type, and the surface condition.

The surface effects of ions were found to be similar to those produced by chemical treatments except that the surface charge induced by the ions was unstable. The effects of positive ions could be counteracted by exposure to gases, such as O_2, which tend to produce a negative surface charge but were little affected by those, such as NH_3, which produce a positive surface charge.

At the termination of the discharge, the excess current recovered as shown in curve (a) of Fig. 10. It was found that heating or exposure to ultraviolet radiation accelerated tbe recovery rate. Exposure to electrons caused an instantaneous decrease in I as shown by curves (b) and (c), Fig. 10.

Estrup proposed that the accumulation of surface charge results from two competing processes, a buildup and a simultaneous decay of charge. The charge on the surface increases until the two processes reach equilibrium. The charge buildup results from the impinging ions depositing charge in surface sites. From the details of the investigation,

Estrup estimates that an impinging ion has about a 10^{-4} chance of creating a charged surface site. These sites are presumably connected with some type of surface imperfection such as a chemical impurity, since clean surfaces or surfaces with only a few layers of "pure" oxide do not show the surface effects. The decay of surface charge is apparently determined by the transport of electrons from the space charge layer to the surface. The transport of electrons, and hence the recovery process, is sensitive to heat, light, and exposure to bombarding electrons.

If a Si surface which had been "recovered" by exposure to electrons was subsequently exposed to positive ions, the current rapidly increased as indicated in curve (d), Fig. 10. The increase was found to be much more rapid than the normal increase indicated by curve (e). Estrup explained this "memory" effect as resulting from a two-step decay process. A charged site decays to a neutral but active site and may remain in this condition for some time before decaying to a normal site. It is easier to charge these active sites than to charge originally the normal sites, hence a surface once charged will "remember" its condition for a considerable length of time. This memory effect is quite important and is also seen in irradiated transistors.

4.4 *General Effects of Radiation on Nonpassivated Devices*

A discussion of radiation effects on semiconductor devices is complicated somewhat by the wide variety of responses found for various devices. Even two supposedly identical transistors may behave quite differently when exposed to radiation. When different manufacturing processes and different experimental procedures are added, the task of extracting a useful picture of the processes involved becomes more difficult. However, it is possible to make some rather broad statements about surface effects of radiation on devices. The predominant effect of irradiation appears to be the formation of channels on the device surfaces which lead to degradation of the device characteristics. The process by which such channels are formed is essentially that studied by Estrup and is due to ions produced in the ambient which diffuse or drift under the fields arising from junction reverse biasing to the semiconductor device surface. Generally speaking, surface effects become noticable at radiation doses $\approx 10^3$ rads (the units of radiation commonly used in surface effects studies are defined in Appendix A) as compared to $\approx 10^7$ rads for bulk effects. Generally, the surface effects saturate at doses $\approx 10^7$ rads. (Saturation has been observed at doses as low as $10^3 - 10^4$ rads in lightly doped particle detectors.)[36] The most radiation-sensitive parameters have been found to be the reverse-bias

leakage current for diodes and I_{CBO} and h_{FE} for transistors. These parameters usually degrade when the device is exposed to radiation although in some isolated cases they have been observed to improve.

For diodes the leakage currents may increase as much as several orders of magnitude and may or may not saturate. The collector leakage current, I_{CBO}, for transistors shows a similar behavior. Transistor gain, h_{FE}, generally decreases with dose and may, at sufficiently large doses, drop below unity. It is frequently found that the degraded characteristics show partial and sometimes complete recovery. Apparently, recovery is promoted by baking, forward biasing, and exposure to radiation without bias.

It is important to note that semiconductor devices operated at low injection levels, such as transistors used in low-level logic, are inherently more sensitive to surface conditions and hence are the most susceptible to surface effects due to radiation. Devices operated at high injection levels, on the other hand, are relatively less affected by surface effects of radiation.

4.5 *Radiation Effects on Diodes*

The amount of work done on nonpassivated diodes which may be discussed in terms of the surface effects of radiation is rather limited. Nevertheless, some interesting effects have been observed on diodes and deserve a discussion at this point.

Freyer[19] and Verrelli[20] have performed the most comprehensive experiments on the surface effects of ambient and radiation on diodes. Freyer subjected Ge diodes, both with and without encapsulation, to Co^{60} gamma irradiation. For the encapsulated devices he found an increase in reverse-bias leakage current during irradiation; he attributed this to bulk ionization which increased the bulk reverse current. To determine the effects of the ambient, he etched the surfaces of decapsulated devices and irradiated them in a controlled atmosphere. The results are indicated in Fig. 11.

Two points are apparent from Fig. 11. First, the magnitude of the reverse current, I, depends on the ambient, i.e., on the relative humidity. As seen in the figure, the reverse current decreases as the relative humidity increases from 0 percent (dry oxygen), passes through a minimum (10 to 35 percent relative humidity), and then increases steadily as the relative humidity approaches 100 percent. Second, at low values of the relative humidity the reverse current increases initially with voltage, reaches a peak at some critical voltage, then drops rapidly to a lower value and remains almost constant for further increases in voltage.

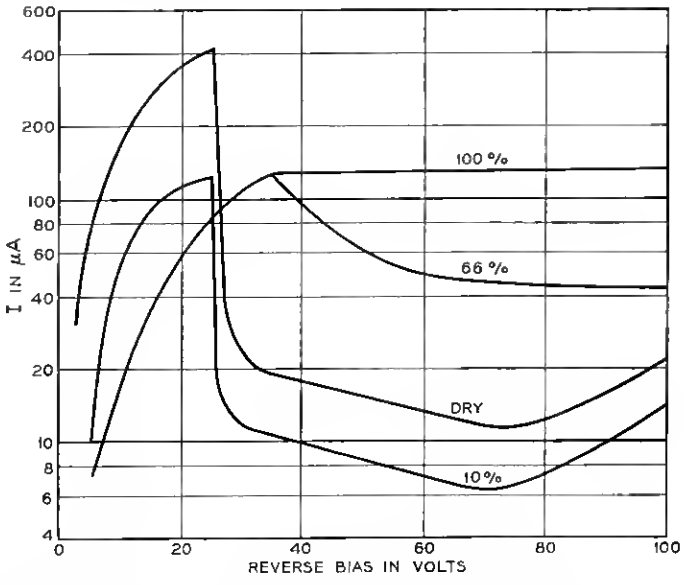

Fig. 11 — Reverse current-voltage characteristics in dry ambient and 10, 66, and 100 percent relative humidity during irradiation (after Freyer, Ref. 19).

Similar results were also obtained by Verrelli under somewhat different experimental conditions, and thus confirm Freyer's observations to be the results of surface rather than procedural effects. Both Freyer and Verrelli explain their results as follows: A Ge diode surface is presumed to be covered with a few layers of oxide which give rise to slow acceptor surface states. In a dry ambient these states are unoccupied, but irradiation causes ionization which supplies electrons to the states. The resultant negative surface charge causes channel formation on the n side of the diode with an accompanying increase in reverse current. If the relative humidity increases, moisture forms on the surface of the diode; this tends to produce a positive surface charge and reduce channel formation and hence the reverse current. As the relative humidity increases to 100 percent, the net surface charge becomes positive because of further moisture collection and a channel now forms on the p side of the junction. The result is an increase in the leakage current.

The peak in the reverse-bias I–V characteristics for dry ambients can be explained in terms of a different mechanism. Verrelli proposes the model shown in Fig. 12. As the reverse-bias voltage is increased, the electric field at the surface near the junction increases and, at some critical value, becomes strong enough to cause desorption of the negative

surface ions, Fig. 12 (b). With the surface charge removed, the inversion layer near the junction is removed and the channel is pinched off, Fig. 12(c). The reverse current, of course, decreases substantially when the effect of the channel is removed.

Estrup[21] investigated the effects of electron and positive ion bombardment on reverse-biased, nonpassivated n^+-p diodes. He found that bombardment with positive ions produced a reverse current-voltage characteristic similar to curve 1 of Fig. 13. According to Buck[22] this type of behavior results from inversion layer (i.e., channel) formation on the diode surface and the resultant effects on leakage current and breakdown described in Section 3.1. A channel is to be expected here since the positive ions produce a positive surface charge which strongly affects the high resistivity side of the p-n junction, in this case the p side, and causes the formation of an inversion layer. A subsequent electron bombardment of sufficient duration should result in a negative surface charge

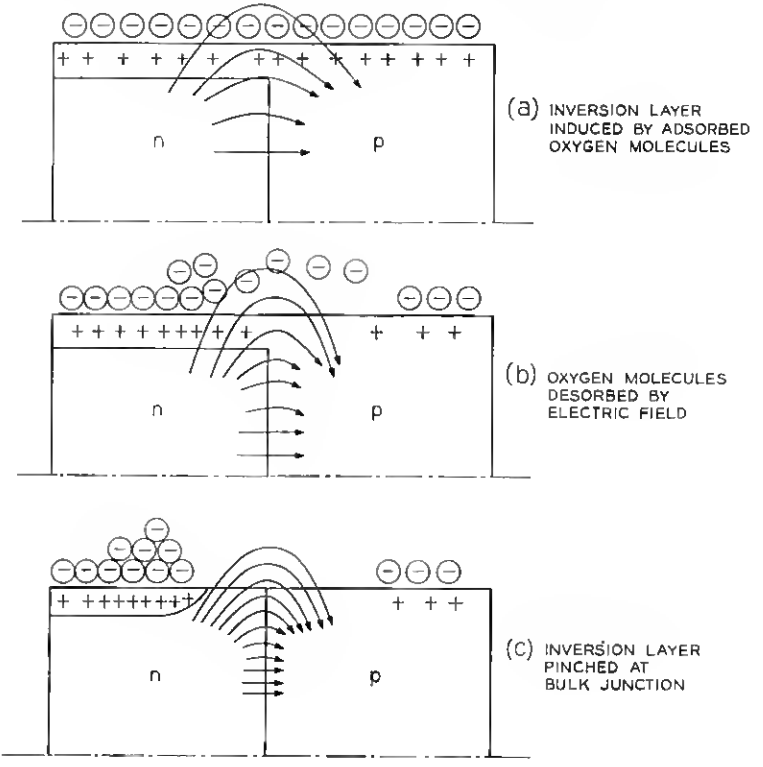

Fig. 12—Proposed model for desorption (after Verrelli, Ref. 20).

and hence an accumulation layer on the p side. Buck predicts for this case a reverse current characteristic as shown by curve 2 of Fig. 13. Estrup did, in fact, observe the predicted change in the characteristic when the diodes were irradiated with electrons. These observations are consistent with Estrup's findings discussed earlier and furthermore support the model for surface effects of radiation on transistors which will be described in the next section.

4.6 *Model for Nonpassivated Transistors with Gas Ambients*

A model which qualitatively explains many of the experimental observations of radiation effects on gas-encapsulated semiconductor devices has been developed by Peck et al.[23] Their model describes the degradation of transistor parameters in terms of the surface inversion layers and channels caused by ionized ambient gas.

This model is best discussed by referring to a typical nonpassivated transistor, as shown in Fig. 14. The device itself is enclosed in a can and surrounded by a gas. The basic process of degradation is explained as follows: Upon exposure to radiation, the gas in the can becomes ionized, and the ions are attracted to the device surface by the electric field created by the collector junction reverse bias and by fields which may exist between the device and the can. As a result, the surface becomes charged either by absorption of the ions onto the surface or by the process, proposed by Estrup,[18,19] of charge transfer from the ions to surface impurities already present. The surface charge layer thus created causes an inversion layer in the region of the collector junction which leads to device degradation.

The model proposed by Peck et al can be elaborated to give a some-

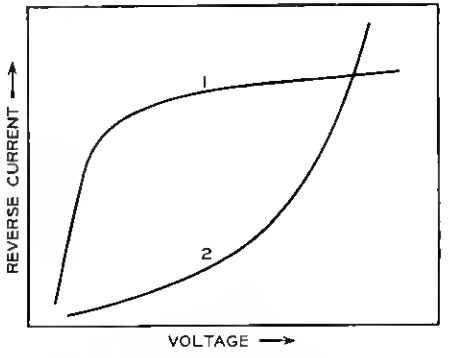

Fig. 13—Schematic representation of diode characteristics. Type 1 = inversion layer, Type 2 = enhancement layer (after Estrup, Ref. 21).

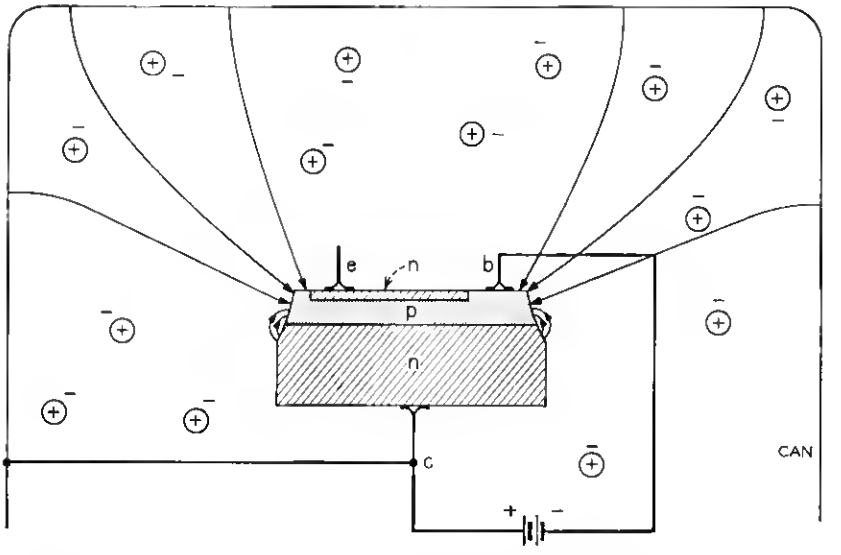

Fig. 14—Cross section of a typical nonpassivated transistor (after Peck et al, Ref. 23).

what more detailed description of degradation. Consider Fig. 15, which shows channel formation on npn and pnp devices in more detail. For the npn device, Fig. 15(a), the channel is shown extending part way from the collector to the emitter while the base surface near the emitter is depleted. Since, by design, the base width of a transistor is quite small, the change in the collector junction area due to the channel will not be sufficient to cause a large increase in I_{CBO} unless breakdown through the narrow depletion layer of the induced p-n junction occurs.[9] However, the positive surface charge near the emitter-base junction will alter the surface potential and hence the surface recombination velocity may be increased resulting in a decrease in h_{FE} .

If the channel should extend across the entire base surface from the collector to the emitter, the surface recombination would be reduced (because the concentration of holes would be greatly reduced). However, a large increase in I_{CEO} would obviously result. Under these conditions, h_{FE} may actually appear to increase since the increase in I_{CEO} would appear as an increase in I_C without a corresponding increase in I_B .

As pointed out in Section 3.2, changes in h_{FE} and I_{CEO} could also arise from changes in generation and recombination at the surface of the base or transition regions. For most devices, however, these effects

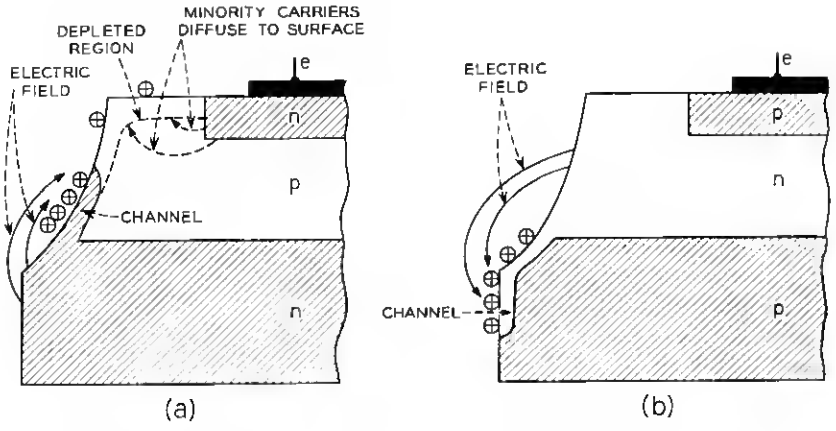

Fig. 15—Channel formation on (a) npn, (b) pnp transistors by positive surface charge.

are believed to be small compared to the effects resulting from channel formation.

For a pnp device, Fig. 15(b), the positive surface charge will create a channel on the collector surface. The area of such a channel may be quite large and cause a significant increase in I_{CBO} because of the increased area of the junction. On the other hand, recombination at the base surface should be relatively unaffected and consequently h_{FE} should be comparatively stable.

It should be pointed out that the above predictions are necessarily of a general nature. While irradiated devices will follow the general pattern of degradation, the detailed behavior of a specific device will depend upon such factors as the device geometry and surface treatment received during fabrication.

Estrup[21] has verified the essential correctness of this model by a series of experiments on Si npn transistors in which he exposed the devices under reverse bias to positive ion and electron bombardment. The effect on I_{CBO} is shown in Fig. 16. The positive ion bombardment starts at point a and continues to point b. During this time, I_{CBO} increases more than two orders of magnitude. According to the model, the ions deposit a positive surface charge on the p-type base of the transistor. This surface charge creates a channel from collector to emitter, which in turn causes the increase in I_{CBO} . From points b to c the device is under no bombardment and a partial recovery is observed, presumably due to some neutralization of the positive surface charge. At c an elec-

tron bombardment begins and, as expected, the positive surface charge is rapidly neutralized, returning I_{CBO} to its original value.

4.7 *Effects of Radiation on I_{CBO} of Nonpassivated Transistors*

Fig. 17 gives an indication of typical results obtained for I_{CBO} degradation of several transistor types exposed to Co^{60} gamma radiation.[24] It should be kept in mind that these curves are only indicative of results found for the types indicated and that the curve for a given device may depart markedly from the curve shown. Inspection of the curves reveals several important facts. As expected, Ge devices have higher initial reverse leakage currents than do Si devices and these currents remain higher, for most cases, up to quite large radiation doses. The magnitude of the I_{CBO} change depends on the device fabrication process (e.g., alloy vs diffused and epitaxial mesa vs mesa) and most

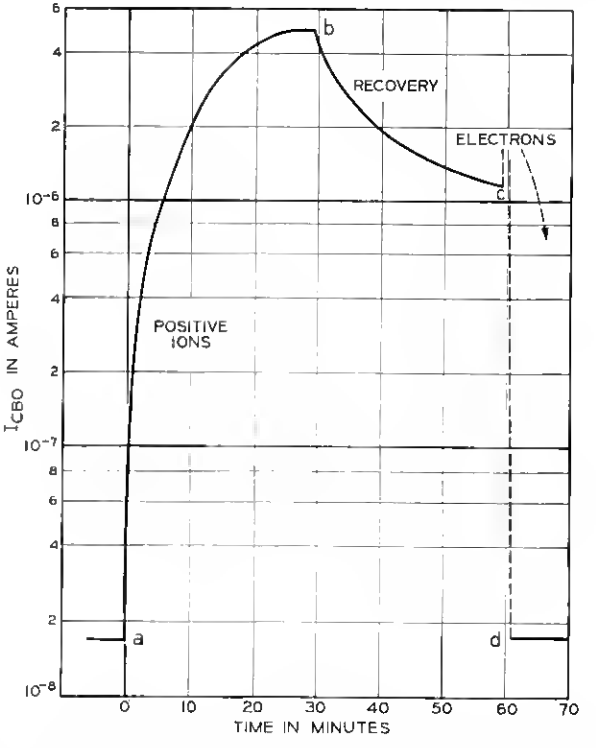

Fig. 16 — Normal effect of positive ions and electrons on a transistor: a-b = discharge on, positive ions drawn to surface; b-c = discharge off; c-d = discharge on, electrons drawn to surface (after Estrup, Ref. 21).

importantly, upon the ambient in the transistor can (e.g., gas-filled vs evacuated).

4.8 *Dose Rate and Saturation Effects*

It has been found that Ge pnp transistors show a saturation of I_{CBO} with increasing radiation dose.[25,26] Furthermore, it appears that the saturation value of I_{CBO} may be dose-rate dependent.[25] On the other hand, a decrease in I_{CBO} for two Ge npn devices has been reported.[26] The improvement appeared to be permanent with I_{CBO} decreasing to one-half its original value. Blair[27] has reported I_{CBO} measurements on a Ge mesa transistor which showed no signs of saturation up to a dose of 10^7 rads. The results for Si transistors are somewhat different from

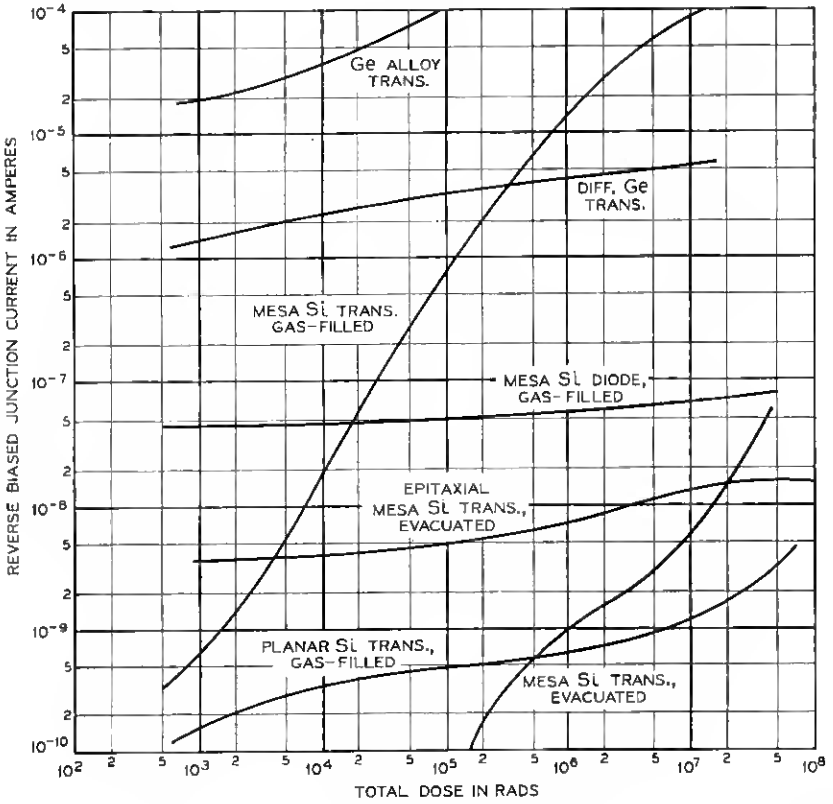

Fig. 17—Typical results for I_{CBO} degradation of several transistor types (after Peck and Schmid, Ref. 24).

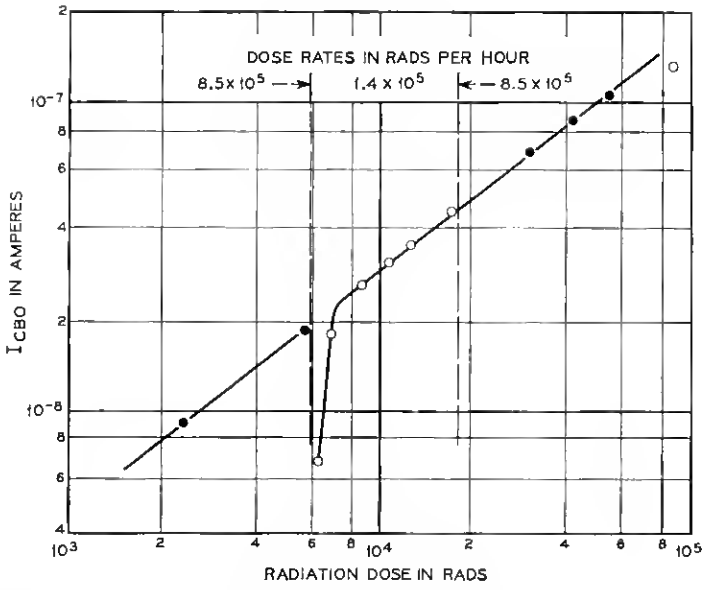

Fig. 18—Reciprocity of dose rate and time at two high radiation dose rate levels (after Peck et al, Ref. 23).

those for Ge in that there is usually no tendency for I_{CBO} to saturate with increasing dose.[26] Saturation has been observed in grease-filled Si transistors.[28]

On the basis of the proposed model, it is to be expected that as the total radiation dose received by a device increases, the number of ions which have reached the device surface will also increase. As a result, the charge accumulated on the device surface and hence the degradation is expected to be, at least approximately, proportional to the total radiation dose. To some extent Peck et al[23] observe this dependence through a reciprocity of dose rate and time for dose rates not too different in magnitude, as shown in Fig. 18. Reciprocity is also observed at dose rates as low as 5 rads/hr.

There are, however, reasons why the degradation should not necessarily follow this simple dependence on total dose. Devices do show recovery, so there must be some leakage process at the surface which counteracts charge accumulation. Recovery, however, usually takes place at rather slow rates and it is likely that at all but very low dose rates such leakage processes are negligible. At sufficiently high dose rates, on the other hand, it is possible that virtually all the ambient

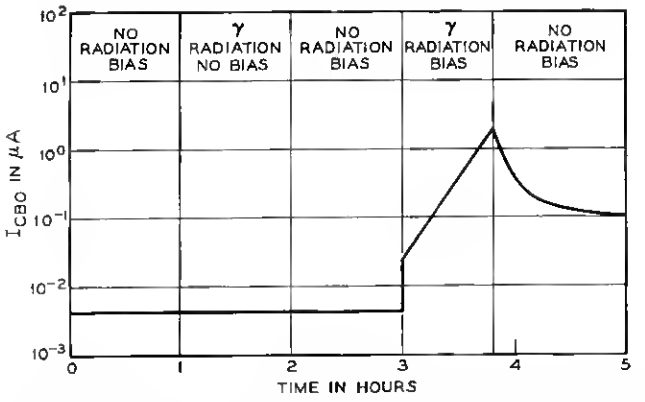

Fig. 19 — The response of I_{CBO} of a diffused Si transistor to either radiation or bias alone or both together. Radiation dose rate 8.5×10^5 rads/hr. (after Peck et al, Ref. 23).

gas atoms are ionized and a further increase in dose rate will not cause a corresponding increase in the rate of degradation.

A saturation effect is also expected from the model discussed above. There is a limit on the amount of charge which can be accumulated on the device surface, because of the limited number of slow states available or the electrostatic repulsion of additional incoming ions. When this point is reached, the degradation will saturate.

Both dose rate and saturation effects are inherent in the model, but, at present, there are too many variables which could influence these effects to allow even qualitative predictions. It is impossible, for instance, to explain why Ge transistors (particularly pnp) show saturation of I_{CBO} while Si transistors, in general, do not.

4.9 *Effect of Bias and Can Potential*

Since the electric fields created by the collector junction bias are intimately involved in the degradation process, one should expect the increase in I_{CBO} to be strongly dependent on applied bias. Experimentally, it is generally found that nonpassivated devices experience degradation only when subjected simultaneously to radiation and reverse bias on the collector junction. The necessity of the combination was pointed out by Peck et al.[23] Fig. 19, which schematically illustrates their results, shows that separately neither bias nor irradiation produces degradation; in combination, however, severe I_{CBO} degradation is produced. The effect of bias voltage is further illustrated in Fig. 20,

which shows the increase in I_{CBO} with dose for various collector biases.[23] Also, it has been shown that if the bias voltage is raised while a device is under irradiation, the rate of increase of I_{CBO} will become larger.[29] If the bias voltage is subsequently returned to its original value, the rate of increase of I_{CBO} will be reduced to the corresponding value.

Another electric field which might be expected to influence the behavior of an irradiated device is the field between the semiconductor and the encapsulating can. Results have been obtained by Peck et al[23] with a Ge transistor whose can-to-semiconductor potential was periodically reversed during irradiation. The increase in I_{CBO} was substantially enhanced when the can was positive with respect to the semiconductor. This result would seem to indicate that positive gaseous ions generated in the gas ambient were responsible for depositing charge on the device surface. This method of surface charge accumulation is in agreement with the model outlined above. Peck points out, however, that lack of reproducibility of results leaves this point open to question. Nevertheless, the can-to-semiconductor potential is important.

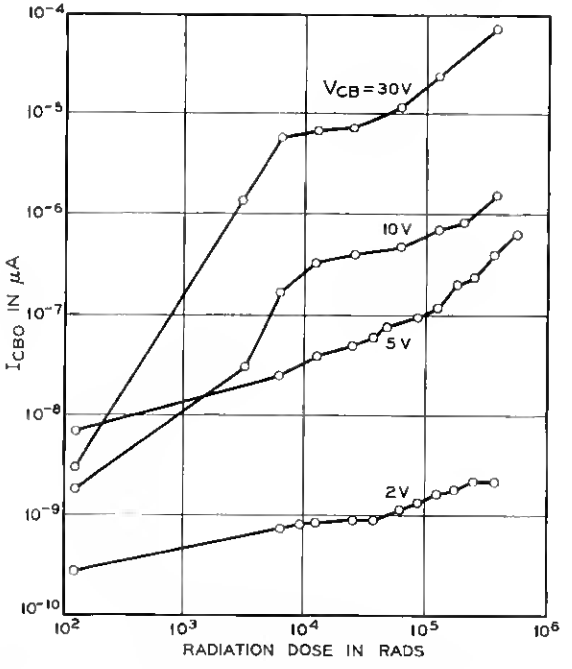

Fig. 20—Dependence of I_{CBO} degradation on collector bias (after Peck et al, Ref. 23).

4.10 *Recovery*

From the model, one would expect a transistor to show recovery of I_{CBO} degradation under certain circumstances. Redueing the bias and hence the electric field at the junction should release the charge trapped on the surface and allow it to disperse. The presence of radiation with the bias removed should further enhance the recovery rate by providing electrons to help remove the positive surface eharge.

Experimentally, the degraded I_{CBO} shows various rates and degrees of recovery depending on several factors. The effects of bias and radiation on recovery rate of gas-filled Si transistors, as reported by Blair,[27] are shown in Fig. 21. In part A of the curve, the transistor has been removed from radiation but is still under bias. When the bias is removed (part B), the rate of recovery is increased, but upon reapplieation of the bias (part C), the recovery rate is again reduced. The most rapid recovery is achieved (prior to parts D, E, and F), if the device is irradiated at 0 volt bias.

Although I_{CBO} usually appears to recover its original value after a sufficient length of time, it is found that subsequent, relatively small doses of radiation will bring I_{CBO} rapidly back to its previous high value. This so-called memory effect is illustrated in Fig. 22 for a device irradiated after one month of shelf recovery time.[27] Apparently the re-

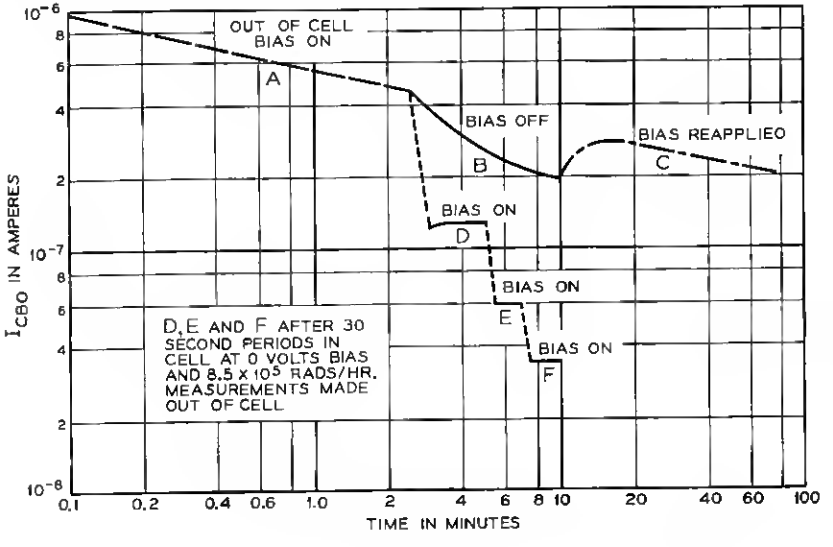

Fig. 21 — Influence of bias and radiation on I_{CBO} recovery (after Blair, Ref. 27).

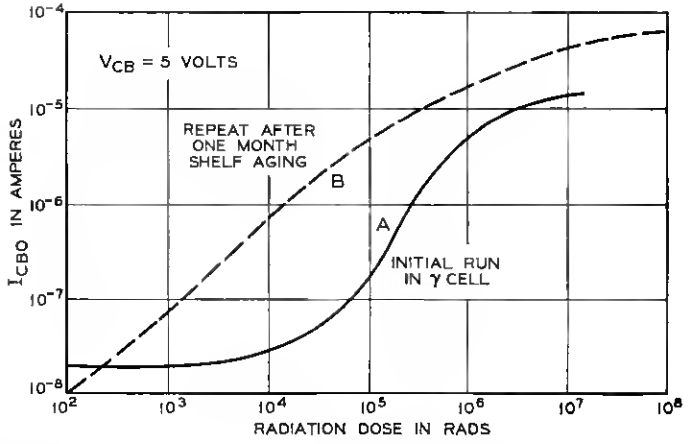

Fig. 22—Si transistor "memory" of radiation after annealing at room temperature (after Blair, Ref. 27).

covery was only superficial and some part of the original damage was still present. Blair reports that even after an additional 15 months of aging the memory effect persisted. However, several authors report the memory effect can be eliminated if the devices are exposed to elevated temperature ($\gtrsim$100°C).

This memory effect is quite similar to that mentioned above in the work of Estrup for Si exposed to positive ion bombardment (see Fig. 10). Estrup suggested that the effect was caused by a two-step discharge process which left the surface states in an "active" but uncharged condition for long periods of time before returning to the normal condition. Estrup offered no elaboration on the nature of these "active" states. However, the fact that the memory can be eliminated by rather small increases in temperature would indicate that the cause of the effect is some small difference between "active" and normal states which anneals out easily.

4.11 *Dependence of Surface Effects on Radiation Type*

Since the primary effect of the radiation is ionization of the gas in the transistor can, it would seem likely that the degradation should be independent of the type of radiation. Peck et al[23] have compared the effects of Co^{60} gamma rays and 18 MeV protons and find that the radiation dose is significant, but can discern no great difference between the effects of the two types of radiation.

4.12 *Effects of Device Ambient*

Many manufacturers attempt, for various reasons, to control the nature of the device ambient by using vacuum, various types of gases, or greases inside the can. These ambients, while in some cases performing the function of passivation, are not an integral part of the device surface and should not be confused with passivation techniques to be discussed later. Although the model discussed previously treated a gaseous ambient specifically, the same general approach should be applicable to other ambients.

The model should be most easily extrapolated to the case of a vacuum ambient. One would expect a marked decrease in radiation sensitivity for this ambient since gaseous ions are no longer present to create a surface charge. Fig. 23 shows a comparison between gas and vacuum ambients for two types of device.[23] As expected, the evacuated devices are less sensitive to radiation.

The situation with grease-filled cans is somewhat more uncertain, and the simple model put forward above would require some refinement to account for the observations. Steele[25] reports that for Ge pnp alloy transistors the presence of silicone grease increases I_{CBO} degradation over values found for the same transistor without grease.

For Si grown junction npn transistors encapsulated in a silicone grease, on the other hand, I_{CBO} was found to saturate with dose, and the saturation value was significantly smaller with grease present. Infrared transmission studies of the grease from Ge devices before and after a 5×10^7 roentgen radiation dose showed that irradiation caused an increase of available hydrogen bonds which were presumably able to interact with the surface. The mechanism causing the change in radiation sensitivity would thus appear to be a surface one, but the reason for the opposite effect on Ge and Si devices is not clear.

A saturation effect for I_{CBO} for silicone grease-filled Si alloy transistors has also been reported by Peck et al.[23] In fact, it was found that I_{CBO} decreased with dose after reaching a maximum. These devices, when exposed to short periods of high intensity radiation, showed only minor changes in I_{CBO}, but showed severe degradation in the periods subsequent to irradiation. These results might indicate production of ions in the grease which require time to migrate to the device surface.

It has been reported that silicone grease also decreased the radiation sensitivity of one type of Si grown junction transistor.[30] After a study of several types of transistors and various case fillings, however, no direct correlation was found between the presence or absence of grease and sensitivity to radiation.

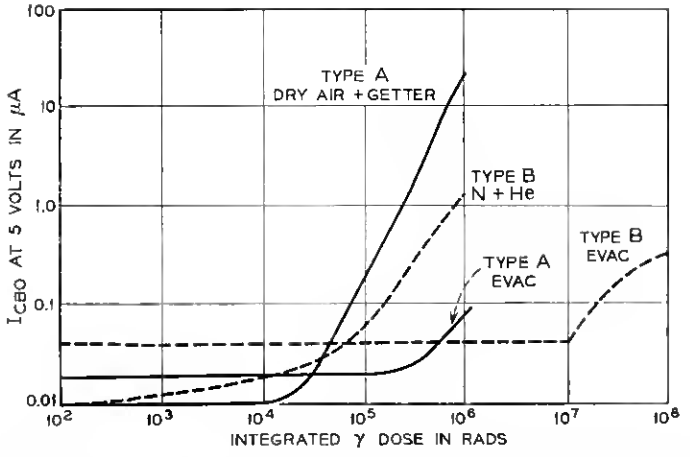

Fig. 23—Radiation degradation of I_{CBO} of two types of diffused Si transistors, evacuated or with gas filling. Radiation dose rate 8.5 × 10^5 rads/hr (after Peck et al, Ref. 23).

4.13 *Effects of Radiation on h_{FE}*

As has been noted, the principal measurements of surface effects of radiation on nonpassivated transistors have emphasized I_{CBO} changes. Because the changes in other transistor parameters are much smaller, they have, to a large extent, been neglected. As will be seen later in the case of passivated transistors, changes in current gain and I_{CBO} are comparable, and studies of changes in other transistor parameters are more extensive. The effects of radiation on transistor parameters other than I_{CBO} in nonpassivated devices have been studied by Zagorites et al.[26] They found for both npn and pnp Si devices a negligible change in h_{FE} for Co^{60} gamma doses up to 1.3 × 10^4 rads. For Ge devices, on the other hand, the changes in h_{FE} were quite large and somewhat erratic. Fig. 24 shows the change of h_{FE} for three npn transistors. In each case the gain decreased by about a factor of two, although the authors claim h_{FE} for some other npn devices increased by the same factor. The changes in h_{FE} correlated strongly with changes in I_{CBO}, and Zagorites suggests that this is evidence for a common mechanism of degradation for h_{FE} and I_{CBO}. On the other hand, h_{FE} for pnp Ge transistors showed both increases and decreases, with no clear pattern emerging.

4.14 *Telstar® Experiment*

Perhaps the best-known example of radiation-induced surface effects on semiconductor devices occurred when the command circuits of the

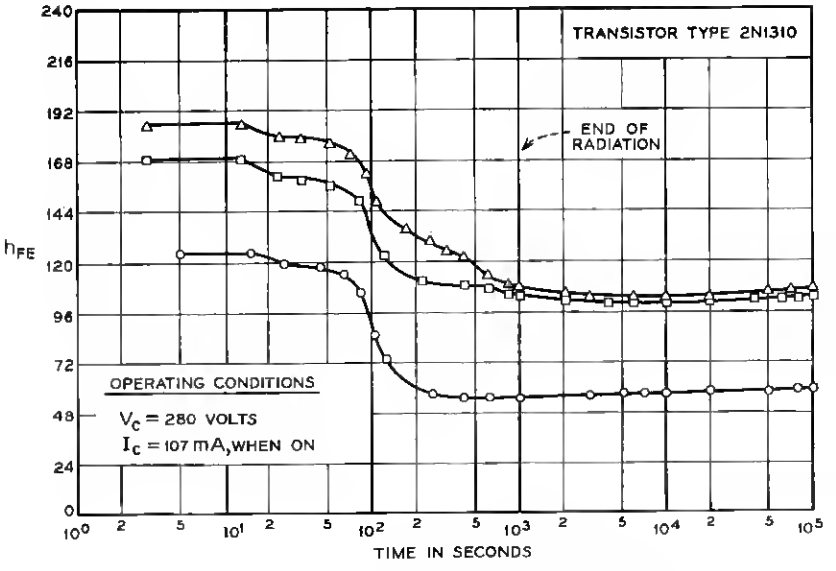

Fig. 24—h_{FE} vs time for three npn transistors (after Zagorites et al, Ref. 26).

Telstar® satellite failed in November 1962.[1] After about four months of successful operation in orbit, the satellite gave indications of serious trouble in the command decoder, and within a few days the circuits failed completely. The maximum radiation dose rate ($\approx 10^3$ rads/hr) seen by the satellite was $\approx$100 times greater than anticipated, probably as a result of a high-altitude nuclear explosion in July, 1962. Several possible causes of the failure were considered and all except surface effects due to radiation on the transistors were ruled out because of lack of supporting evidence or correlation with the observed failure symptoms.

In an effort to discover more about the effects of ionizing radiation on the command circuits, circuits similar to those used in the satellite were cycled between high and low dose rate Co^{60} gamma radiation with the same period as that of the satellite in the radiation belts. The radiation-sensitive transistors in these circuits were nitrogen-encapsulated, diffused Si types. The transistors in the circuits showed the expected response to radiation, i.e., I_{CBO} and h_{FE} degradation at high dose rates followed by some recovery at low dose rates. The recovery was enhanced by reduction of bias, especially if the dose rate was high. A wide range of memory effects was also observed. Failure in one irradiated

circuit was traced to h_{FE} degradation of one transistor, while failure in another circuit was attributed to an I_{CBO} increase.

After a careful analysis of these laboratory tests, attempts were made to rejuvenate the *Telstar*® satellite circuits. Several unsuccessful attempts were made using various approaches. Finally, success was achieved with modified commands designed to circumvent one particular circuit which was assumed to have failed. The satellite then responded to subsequent commands and after some further manipulation the circuits were fully operational.

The exact reason for recovery is not known but was probably a combination of two effects. First, the dose rate seen by the satellite had decreased significantly from the value which first produced failure, with a consequent decrease in surface effects. Second, the suspected circuits were given a series of continuous commands. This manner of operation caused the normally off transistors (high V_{CE} and high rate of degradation) to have a decreased average bias voltage. Under these conditions, the surface degradation is decreased and recovery proceeds more rapidly.

4.15 *Miscellaneous Nonpassivated Devices*

4.15.1 *Introduction*

The discussion thus far has been limited to transistors and diodes. However, other semiconductor devices, not necessarily junction devices, are also sensitive to surface effects and are just as likely to be exposed to radiation. Unfortunately, there has been very little investigation of these devices, at least as far as surface effects of radiation are concerned.

4.15.2 *Solar Cells*

Solar cells will be exposed to radiation mainly in space applications, and studies of radiation effects on these devices have been made with these applications in mind.[31,32,33,34] Results obtained by Rosenzweig et al[34] indicate that the Si n/p cells presently used are most likely to degrade from bulk rather than surface radiation damage because most of the minority carrier generation in these devices takes place well below the surface. The importance of bulk damage is illustrated in Fig. 25, which shows the percent quantum efficiency as a function of wavelength for an n/p Si solar cell after various doses of 1 MeV electrons. It is evident that the efficiency is most affected at the longer wavelengths, those at which carrier generation occurs well below the surface, i.e., in the bulk damage region. It should be pointed out that similar optical

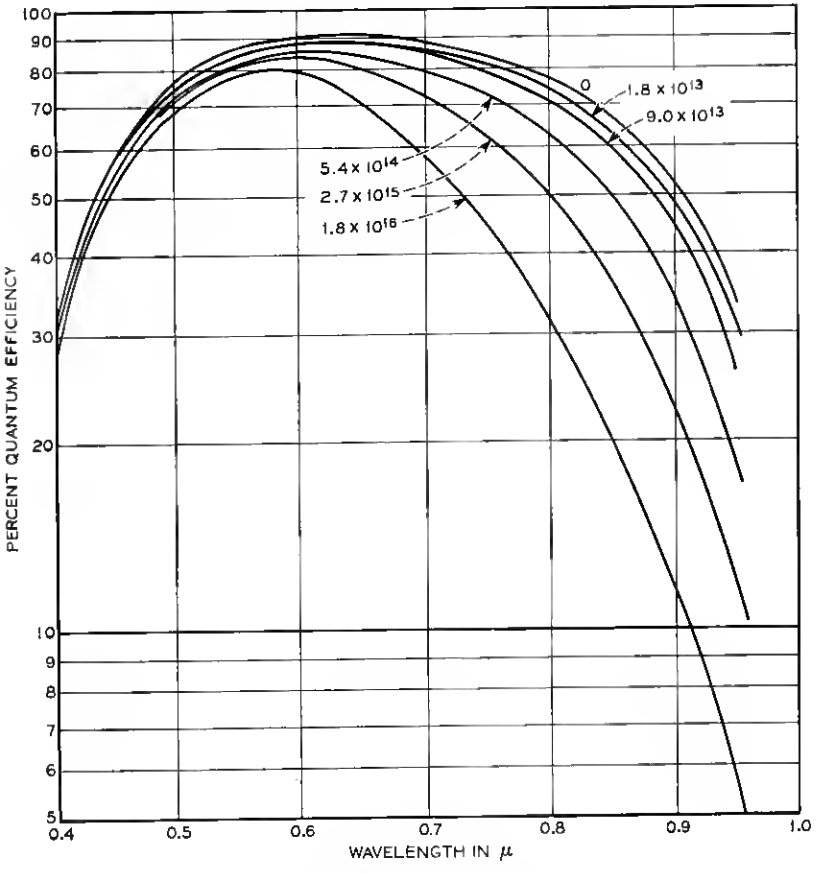

Fig. 25 — Percent quantum efficiency vs wavelength after various levels of bombardment for n/p cells (after Rosenzweig et al, Ref. 34).

studies could be quite useful for investigating surface effects in other semiconductor devices. In particular, they can be used to distinguish between surface and bulk effects as illustrated here for solar cells.

There has been recent interest in GaAs solar cells, since these devices approach Si solar cells in conversion efficiency and may, for some applications, be more radiation resistant.[31,35] Minority carrier generation near the surface is more important for GaAs solar cells, however, and it is possible that changes in surface recombination due to radiation are important on these devices.

4.15.3 *Radiation Detectors*

Radiation detectors in the form of specially designed reverse-biased diodes require stable surface properties to keep the noise level as low as possible.

Detectors used in *Telstar*® satellites used bare, etched, diffused *p-n* junctions inside a tight can back-filled with nitrogen containing a trace of oxygen. It was found necessary to add the trace of oxygen to stabilize the diodes against gradual increases in reverse current.

These detectors were tested for surface effects due to radiation by exposing them to 50 rads/hr gamma radiation while under intermittent reverse bias. The devices showed a wide range of responses as observed in reverse current measurements. However, none of the devices showed serious permanent effects due to irradiation. In space, on the other hand, two detectors out of 18 did show significant surface-generated noise after several months of operation at radiation levels higher than expected.

Oxide-passivated surfaces in place of bare, etched surfaces have not been tested for these devices, but based on the experience with passivated transistors one might expect to find problems in the form of charge storage effects at the $Si\text{-}SiO_2$ interface.

4.15.4 *Metal-Semiconductor Junctions and Heterojunctions*

The region of the interface between two materials, such as a metal and a semiconductor, is obviously not a true "bulk" region from a radiation effects point of view since it is a small region not typical of either material. Similarly, it is not a "surface" region in the usual sense of the word. Nevertheless, such interfaces are important and it is worthwhile here to broaden the definition of a surface to include interfaces and to discuss interfaces as they concern radiation effects.

It is difficult to predict what effect radiation will have on an interface region, since little is known about these regions and almost no experimental investigations have been carried out. However, it is known that, at metal-semiconductor junctions and heterojunctions, the crystallinity is either nonexistent or at least badly disturbed. As a result, these regions are likely to contain numerous trapping centers. Radiation may alter the number of these centers or the charge they contain, and hence may alter the characteristics of the device containing the interface. There has been an indication that radiation does affect a metal-semiconductor interface.[37] The saturation current of an Ag surface barrier GaAs varactor was found to *decrease* 10 to 20 times after receiving a

fast neutron dose of $10^{15}/cm^2$. Similar diffused GaAs varactors, on the other hand, showed the more typical increase in the saturation current, presumably caused by usual bulk effects. The unexpected decrease in saturation current of the surface barrier devices, however, is suspected to result from an increase in the barrier height of the interface. Such an increase could result from a change in the charge contained in the interface states as a result of irradiation.

Such radiation-induced changes in the metal-semiconductor barrier height could also affect the characteristics of commonplace p-n junction devices through their many metal-semiconductor junctions. However, no direct study of such effects has yet been made.

V. PASSIVATED DEVICES

5.1 *Introduction*

In recent years Si planar devices have assumed an increasing importance in the transistor industry. There are several advantages of planar devices over other device types such as alloy or mesa. One of these advantages is that the Si planar device lends itself naturally to an oxide surface passivation, which is quite effective in reducing the surface stability problems encountered in other types. At present only Si devices are commercially available with this oxide passivation; a comparable passivation technique for Ge devices is still in the experimental stage. The discussions in this section are understood, therefore, to apply to Si and Si devices.

As far as the effects of radiation on planar devices are concerned, it will be seen that the surface passivation layer itself plays a very important role. For this reason a short discussion of Si surface passivation and its effects on devices will be given to serve as a basis for the subsequent discussion of radiation effects.[38]

The electrical requirements of an ideal passivation material have been given by Young and Seraphim[39] as follows:

(*i*) The semiconductor surface potential must not change significantly with time under the stress conditions that are encountered by the device.

(*ii*) The semiconductor surface potential should be optimum for the particular device under consideration.

(*iii*) In those types of devices which require reasonably small values of the surface charge density and the surface recombination velocity, these characteristics should also be accomplished by the passivation.

The passivation used on planar devices is by no means perfect, but it does approach these ideals reasonably closely.

In practice, passivation of silicon devices is accomplished with a film of the oxide, SiO_2, which is thermally grown on the device surface. Because of the intimate contact between the oxide and semiconductor surface, this film stabilizes the surface and isolates it from the ambient. However, this type of passivation places the surface of the device in contact with a material which interacts in a complicated way with it and with the ambient. It has become apparent that if one is to understand the behavior of passivated devices one must understand the charge storage and transport mechanisms which occur in the thin layer of passivation material.

5.2 *Silicon Dioxide as a Passivation Material*

5.2.1 *Effect of SiO_2 on a Si Surface*

An extensive experimental study of SiO_2 as a passivation material has been made by Atalla et al.[11,40,41] They found that oxides grown at about 1000°C in dry or wet oxygen are continuous, amorphous, and stable over long periods of time. Atalla discussed their observations on the SiO_2–Si system in terms of fast and slow surface states. By using field effect techniques it was found that the passivated surfaces showed no apparent effects due to slow surface states. Furthermore, the presence of either wet or dry nitrogen caused no shifts in the surface conductivity resulting from the introduction of slow surface states.

Atalla reported the presence of fast surface states with densities $\approx 10^{10} - 10^{11}$ cm^{-2} and suggested the following model to account for their presence. At the SiO_2–Si interface, a region of gradual transition from crystalline Si to amorphous SiO_2 occurs, and it is assumed that Tamm-like states exist in this trausition region. These states together with states arising from vacancies caused by mismatch between the Si and SiO_2 are acceptor states. Donor states arise only from the presence of impurities at the interface.

5.2.2 *Charge Storage Effects in SiO_2*

Recent investigations have revealed charge storage effects in SiO_2 films such as those used for surface passivation on Si devices. Yamin[42,43] has studied the charges in tbermally grown SiO_2 films using a Si–SiO_2–metal sandwich. The Si nsed was either n- or p-type, the oxide was typically 6000 Å thick, and the metal was usually Al or Au in the form of a circular dot. Yamin investigated the charge flow in and out of these devices for Si potentials between ±5 volts with respect to the metal at temperatures from 200°C to 400°C. At negative Si potentials, it was observed that the amount of charge entering the device was much

greater than expected from the device capacitance. Furthermore, the excess charge could be recovered if the Si potential was again made more positive, or it could be stored almost indefinitely in the device if the leads were opened. Yamin demonstrated that the charge storage was associated only with the oxide directly under the metal dot and estimated the density to be 4×10^{12} to 2×10^{14} charges/cm^2, depending primarily on the method of preparation of the oxide. Devices which were baked for 15 minutes at 1000°C in dry oxygen, nitrogen or hydrogen showed a spontaneous discharge at 400°C corresponding to charge densities in the oxide of $\approx 10^{12}$ charges/cm^2. Since these devices had not been previously voltage-stressed, it appears that thermally produced oxides may contain a built-in charge. A study of the conductivity of the Si beneath the oxide showed that the conductivity became more n-type, indicating that positive charge was being stored.

Charge accumulation and instability effects in SiO_2 films exposed to elevated temperatures and electric fields have been observed by others[44,45,46,47,48,49] and various mechanisms have been proposed to explain the observations. It is now generally believed that the effects are due to the presence of mobile positive ions in the oxide. Snow et al[44] have observed changes in the capacitance-voltage characteristics of metal-oxide-semiconductor structures under temperature and voltage stress. These observations have been explained in terms of alkali ion (in particular Na^+) transport through the oxide. Using radioactive tracer techniques, Yon et al[50] have observed changes in the Na impurity profile in SiO_2 films which correlated with observed changes in the charge contained in the oxide. Hofstein,[47] on the other hand, has observed similar charge storage effects in SiO_2 but his results suggest hydrogen ions as the mobile positive charge carrier. Furthermore, it has been shown that the presence of hydrogen during the heat treatment of SiO_2 films, either as an ambient gas or as moisture on the surface, has a considerable effect on the behavior of the oxide.[46,47]

Both explanations may be substantially correct, however, since it appears that charge storage effects are very dependent on the conditions of oxide preparation and on subsequent heat treatments.[46] With our present limited knowledge of the processes occurring in SiO_2 one must be very cautious in applying the results of an investigation on one type of oxide to another oxide prepared under different or unknown conditions.

It has been found that a P_2O_5 treatment of the SiO_2 passivation layer reduces the charge storage effect and increases device stability.[52,53,54] Pliskin[55] has suggested that the P_2O_5 treatment increases the poly-

merization of the SiO_2 tetrahedra. The result is a denser SiO_2 layer through which the positive ions have more difficulty diffusing. It has also been suggested that a phosphate glass layer on the surface of the SiO_2 acts as a getter and reduces the effective impurity concentration in the underlying oxide.[54]

5.3 *Electrical Behavior of SiO_2 Passivated Devices*

Atalla[41] has studied SiO_2 passivated p-n junctions under various conditions of bias and relative humidity and has proposed a model which satisfactorily explains his findings. Briefly, he found the reverse leakage current of the junction unaffected by moisture when the junctions were subjected to extended periods of forward or zero bias. For a steady reverse bias, however, the reverse current increased with time and saturated in a few hours at a value of about five times its initial value. The increase in current was a function of relative humidity, bias voltage, and oxide thickness. By optically scanning the junctions, Atalla observed that the increase of reverse current occurred simultaneously with the formation of channels on both sides of the junction.

The following model was proposed by Atalla to explain the above observations. When the SiO_2 surface is exposed to moisture, a layer of water containing mobile ions is formed. When a reverse bias is applied to the junction, an electric field appears at the oxide surface in the region of the junction, Fig. 26(a). This field causes mobile ions on the surface of the oxide to migrate, positive ions toward the p side, negative ions toward the n side. If the charge separation is severe enough, the semiconductor surface near the junction will become inverted and channels will form, Fig. 26(b). It is apparent that the effect depends on the humidity and the field strength at the oxide surface, and in turn on the bias voltage and oxide thickness. As with nonpassivated devices, the channels cause an increase in reverse leakage current.

Failure mechanisms in SiO_2 passivated planar transistors were also studied by Metz[56] who observed changes in the I_{CBO} vs bias voltage characteristics as the devices were aged under operating conditions (emitter junction forward-biased, collector junction reverse-biased). Again, I_{CBO} degradation occurred at elevated junction temperatures, with I_{CBO} increasing several orders of magnitude in some cases. Metz found that the current increases were reversible and that I_{CBO} could be returned to its original value by heating for several minutes without bias or by removing the bias and opening the can, exposing the device to normal ambient atmosphere. The model discussed by Metz is essentially the model proposed by Atalla and satisfactorily explains the

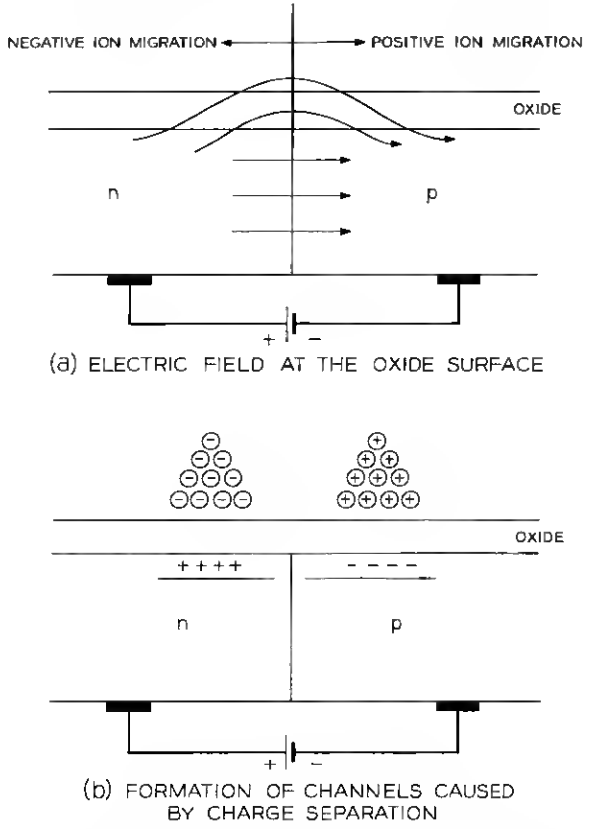

Fig. 26 — Separation of the charge on the surface of a reverse-biased p-n junction.

observed recovery. Heating without bias increases surface ion mobility, and the separated ions redistribute themselves to a neutral condition through their mutual attractiou field. Exposing the surface to ambient atmosphere (and hence moisture) also increases the ion mobility and hence promotes a neutralization of surface charge.

Atalla's model has received support from the work of Shockley et al[57,58] wbo investigated contact potential variations on SiO_2-covered Si surfaces using a Kelvin probe. They were able to account entirely for the observed variations by assuming the presence of mobile charges on the outer surface of the SiO_2 which migrated under the influence of applied electric fields.

In contrast to Atalla's model, in which the surface potential of the device is controlled by charges on the surface of the passivation layer,

the most recent studies indicate that charge storage and transport effects *within* the SiO_2 passivation are responsible for device degradation. Electric fields exist in regions of the oxide near biased junctions and these fields may cause charges within the oxide to accumulate at the Si–SiO_2 interface. Such a charge accumulation would, of course, strongly influence the surface potential of the adjacent Si and lead to degradation by the methods discussed earlier.

This model is supported by the work of Mathews et al[59] who have investigated the effect of Na contamination of the passivation layer on device stability. They concluded that Na ion migration through the oxide was an important cause of degradation of their devices. Snow et al[44] have also suggested that trace alkali impurities in the passivation oxide may cause reliability problems in devices operated at high temperatures and voltages.

Basically, then, it appears that surface conditions in passivated devices can be controlled by two possible mechanisms, charge storage in the SiO_2 layer and charge separation on the surface. However, the first mechanism appears to be the important one in most types of planar devices. Of course, it is possible that under some circumstances both mechanisms may be operative.

5.4 *Results of Device Passivation*

In spite of the problems of charges present in or on the surface of the SiO_2 film, passivation has unquestionably improved the performance of many silicon devices. I_{CBO} values are relatively low and very stable, surface recombination near the emitter junction is low and, consequently, achievable current gains are quite high. Surface recombination velocities as low as 10 cm/s for oxidized Si surfaces have been reported by Grove and Fitzgerald.[60]

Under almost all conditions of preparation, the charges stored in or on the oxide are positive and hence tend to induce n-type surface conductivity in any underlying material. In the case of npn transistors, such surface layers will tend to reduce the collector breakdown voltage and increase recombination in the emitter-base region (i.e., lower h_{FE}). On the other hand, for pnp transistors such surface conductivity results in unstable collector channels and very low recombination at the base interface. Current manufacturing processes for pnp devices stabilize the collector channels with a p^+ diffused guard ring about the collector junction. Because of the low recombination currents in the emitter-base region, passivated pnp transistors have very high h_{FE} values down to very low emitter currents.

5.5 *Radiation Effects on Passivated Devices*

5.5.1 *Introduction*

The question of importance here is, of course, what effect passivation will have on the response of devices to radiation. Unfortunately, although a considerable amount of investigation has been carried out on passivation per se, the amount of work done on the effects of radiation on passivated devices is rather scant. Despite this handicap, however, some facts are fairly well established. In general, the effects observed are quite similar to those observed in nonpassivated devices and seem to be associated again with channels resulting from the formation of ions in the neighborhood of the surface. However, because of the variety of ways in which SiO_2 layers are produced, the nature and charge state of the ions before and after ionizing radiation are not reproducible.

5.5.2 *Experimental Results*

The effects of radiation on diffused planar diodes and npn transistors passivated with 1.3μ of thermally grown oxide followed by 1.3μ of fused lead borosilicate glass have been reported by Kerr.[61] Typical results for the devices, under 20 volts of reverse bias, are shown in Fig. 27. The reverse current appears to saturate at a dose of 10^5 to 10^6 rads, and further investigation showed little change for doses up to 10^8 rads. There is no obvious explanation why the diodes are more sensitive to radiation than the transistors. Kerr also reports recovery of the leakage current degradation in one hour in radiation at a 1.9×10^5 rads/hr dose rate with no bias and recovery in longer periods with bias and no radiation or with no bias and no radiation. This author has also compared SiO_2-protected devices, with similar varnish-protected Si mesa diodes and finds the degradation is about an order of magnitude smaller for the oxide-covered diodes.

Mathews et al[59] have exposed $p\pi n$ diodes, with and without alkali contamination in the glass envelope, to Co^{60} gamma radiation. The results indicated that the presence of alkali atoms considerably enhanced the reverse leakage current degradation. The excess reverse current was found to be associated with channels on the diode surface. These channels were eliminated only when the last of the protective oxide was removed.

The effects of low-energy X-rays (150 keV) on the ac and dc current gains of SiO_2-passivated npn planar transistors have been investigated by Taulbee et al.[62] At such low X-ray energies, atomic displacement effects should be negligible. The degradation of dc gain for three

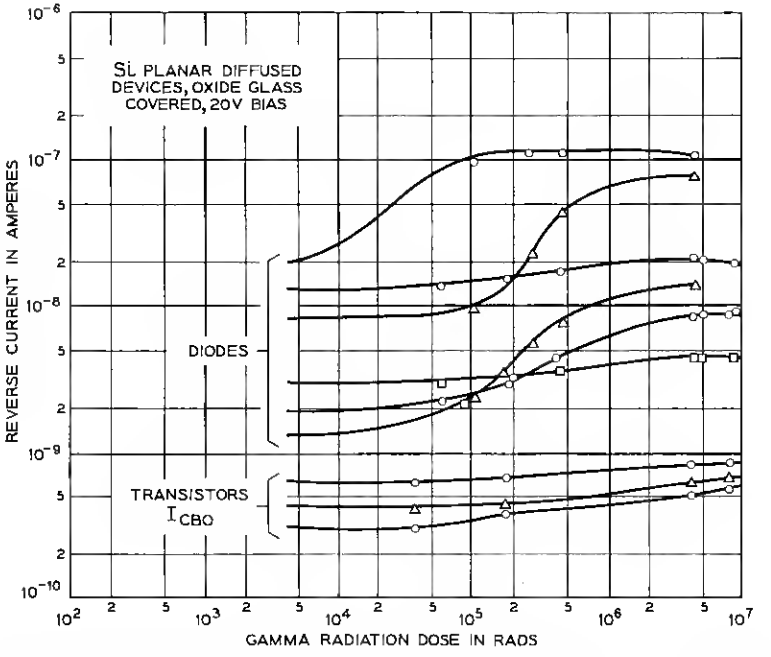

Fig. 27 — Degradation produced by reverse bias and γ-irradiation of oxide-glass covered planar diodes and transistors. Dose rate 1.9 $\times$ 10^5 rads/hr (after Kerr, Ref. 61).

devices irradiated in the passive condition (i.e., with no bias applied to either junction) appeared to saturate at a dose of about 10^7 rads. The effect of the degradation was strongly dependent on the emitter current, I_e, as shown in Fig. 28. In this figure, $1000/h_{FE}$ is shown as a function of I_e for the three devices before and after exposure to 10^7 rads of 150 keV X-rays. The effective degradation is much more severe at low emitter currents with current gains falling to as low as unity at 1 μA.

Taulbee found that the effects were also dependent on junction bias applied during the irradiation. The gain degradation increased if either junction was reverse-biased and decreased if either junction was forward-biased.

The X-ray-induced damage appears to be relatively stable under shelf-life conditions. Over a period of 200 days, the irradiated devices recovered about 20 percent with no significant difference observed between devices with and without cans. Recovery was achieved if bias was applied to the transistor, high values of emitter current producing the most rapid recovery. The amount of damage exhibited by a given type

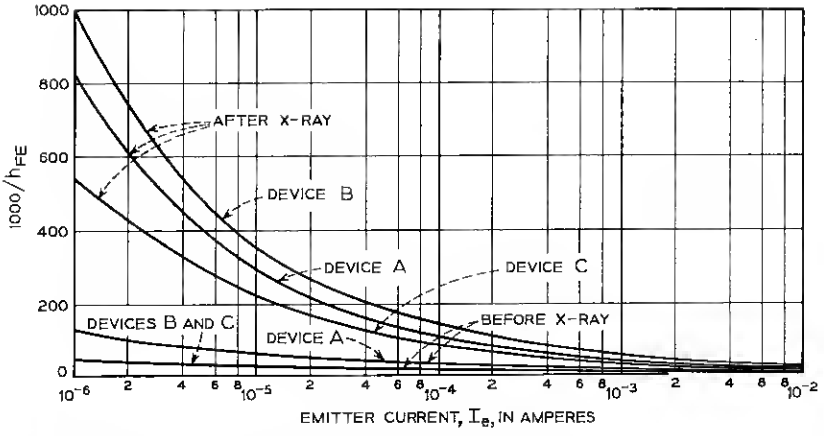

Fig. 28—Dependence of h_{FE} degradation on emitter current after $\approx 4 \times 10^7$ rads x-ray dose. (after Taulbee et al, Ref. 62).

of device appeared to vary with the manufacturer; five lots of the same devices supplied by five manufacturers showed widely varying responses. It is, of course, natural to suspect that the cause is the different surface treatments given the devices by each manufacturer.

An extensive and systematic study of passivated planar devices has been made by Schmid,[63] who finds a predictable pattern of response to Co^{60} gamma radiation for many types. All npn devices exhibit a rapid drop in dc current gain (to as low as 10 percent of the initial value at doses of 10^6 rads) accompanied by a slow increase in I_{CBO}. The pnp structures, on the other hand, show little decrease in gain, but I_{CBO} increases as much as six orders of magnitude at doses of 10^6 rads. In some cases, I_{CBO} saturates and actually recovers slightly with increasing dose. The response of a given device is found to be characteristic of the manufacturer, and it has been shown that changes in the device surface structure will significantly change the response. High-gain devices were found to degrade proportionally faster than devices with low gain.

Contrary to the findings of Taulbee,[62] the h_{FE} degradation was found by Schmid, to a first approximation, to be independent of bias. In fact, the decrease in gain was sometimes greater without bias. Schmid did not examine the effects of reverse emitter bias. Over relatively long periods, the degradation appeared to be permanent under shelf-life conditions. However, a two-hour bake at about 300°C restored the original characteristics, and a second exposure to radiation repeated the previous degradation.

Schmid explained the difference between the behavior of npn and pnp transistors as follows: Ionizing radiation creates a positive charge in the oxide layer or at the oxide-semiconductor interface which affects the base regions of the transistors. For an npn device, the positive surface charge increases the surface recombination at emitter-base region. The result is an inerease in base current required to maintain a given collector current and hence a decrease in gain. For pnp transistors, the positive surface charge creates a collector channel which results in an increased I_{CBO} as discussed previously.

Many of the degradation features observed by Peck[23] on gamma-irradiated nonpassivated device have also been observed by Stanley[64] in high-gain pnp and npn Si planar transistors irradiated with 1.5 MeV electrons. (See Appendix B for a discussion of the dose equivalence of electrons). Tbe degradation was found to be most pronounced in the collector-to-emitter leakage current, I_{CEO}. (Large increases in I_{CBO} for an npn transistor result from channel formation across the base from emitter to collector.) Fig. 29 sbows the I_{CEO} increase for an npn transistor as a function of the total electron dose. It appears tbat I_{CEO} will saturate after increasing several orders of magnitude. It is also apparent that both radiation and bias, V_{CE}, must be present for degradation to occur. During the times AA, BB, etc., when $V_{CE} = 0$, the transistor shows recovery. As with nonpassivated devices, the recovery is much more pronounced when radiation is present (compare DD with EE). Stanley reported that forward-biasing the emitter junction also improved the recovery of the leakage current and in many cases restored I_{CEO} to its preirradiation value.

Fig. 29 also shows evidence of a memory effect similar to that observed by Peck;[23] i.e., after the annealing periods BB, CC, DD, and EE, I_{CEO} returns to its preannealing value very quickly (compared with the overall rate at which I_{CEO} is increasing) as though it "remembered" its previous irradiated condition.

The transistors examined by Stanley also showed h_{FE} degradation under electron bombardment. The degradation was much more severe at low emitter currents, 5 to 10 μA, than at bigher currents, $\approx$1 mA. The final gain at 10^{15} e/cm^2 dose was about the same ($\approx$10) for many units and sbowed no correlation with preirradiation values. One type of transistor encapsulated in a high-density silicone compound did not exhibit such severe gain reduction, presumably because of increased shielding which was able to stop 1.5 MeV electrons. However, two other types of plastic encapsulated transistors showed severe gain degradation at low current.

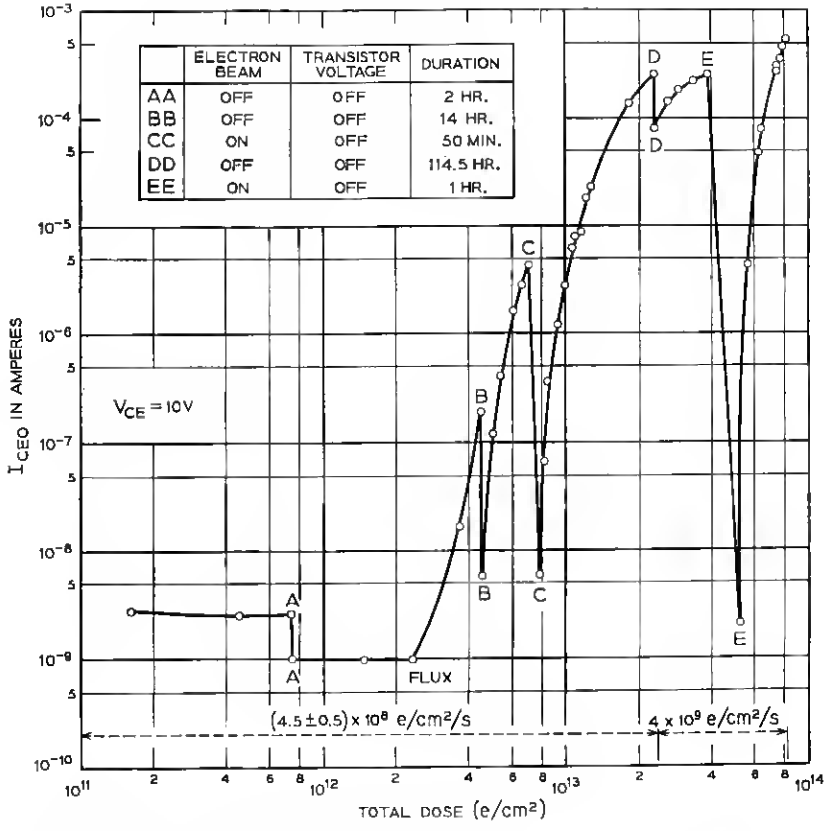

Fig. 29—I_{CEO} vs total electron dose (1965-11 Fig. 2. Lincoln Laboratory, MIT Reprinted by permission) (after Stanley, Ref. 64).

The effects of electrons and Co^{60} gamma rays on the dc gain of npn and pnp Si transistors have also been reported by Brucker et al.[65,66] They found the loss of gain caused by increased surface recombination effects to be nonlinear with radiation dose. By irradiating npn planar transistors with 125 keV and 1 MeV electrons they found

$$\Delta(1/h_{FE}) = K_a\left(\frac{\phi}{I_E}\right)^{\frac{1}{2}} + K_b\frac{\phi}{I_E^{\frac{1}{2}}},$$

where K_a and K_b are the surface and bulk damage constants respectively, ϕ the integrated electron flux, and I_E is the emitter current. The degradation is greater at lower values of I_E as expected from previous discussions. The equation holds for $\phi \leqq 5 \times 10^{14}$ e/cm^2. At larger values

of ϕ the surface component was observed to saturate. Brucker attributes the surface part of the degradation to charge accumulation in the oxide which results in an increase in the surface recombination velocity at the emitter-depletion layer surface. Brucker also reported that the surface effects readily annealed out at 250°C.

For Si planar transistors Hughes[67] has found that a dose of 10^6 rads of Co^{60} radiation can cause I_{CBO} to increase four orders of magnitude and h_{FE} to decrease to 25 percent of its preirradiation values. The response of the devices to radiation was found to be quite dependent on bias conditions but, interestingly enough, independent of whether the ambient was a gas or a high vacuum. This last observation lends support to the view that charges within the oxide rather than on the oxide surface are responsible for degradation. The effect of surface charge was observed to be severe enough to invert even the highly doped p^+ guard ring on pnp transistors. The degradation of h_{FE} and other parameters in both npn and pnp Si planar-passivated transistors exposed to electron beams (5 to 50 keV) has been observed by Green and others.[68] The degradation was found to be reversible in that it could be removed completely by annealing for several hours at 250°C. Partial recovery was observed at lower temperatures. The interesting point in these experiments is that the degradation only occurred when the electrons had sufficient energy to penetrate to the Si–SiO_2 interface; electrons stopped in the oxide away from the interface had no effect. Subsequent measurements with a small scanning light spot showed that the surface recombination velocity had increased in the base region of the transistors.* The minimum electron energy required to cause h_{FE} degradation of npn and pnp Si transistors has been measured by Stanley.[71] He also found that degradation occurred only when the electrons penetrated to the Si–SiO_2 interface.

5.6 *Radiation Effects in Metal-Oxide-Semiconductor Field Effect Transistors*

Field effect transistors are majority carrier or unipolar devices and as such were originally believed to be relatively insensitive to radiation effects because their characteristics did not depend on minority carrier

* Schmidt[69] has suggested for these experiments that the irradiation has interacted in some manner with a hydrogen-containing species (presumably resulting from moisture trapped at the Si-SiO_2 interface when the SiO_2 layer was stream grown) at the Si-SiO_2 interface. Schmidt based this suggestion on his discovery that protons incorporated into anodically grown oxide films on Si cause the formation of a large number of surface recombination centers.[70] The effect in transistors was observed to decrease with more irradiation annealing cycles, perhaps indicating that the limited supply of hydrogen in the oxide was being reduced.

lifetime. The effects of electron irradiation on planar junction field effect transistors have been investigated by Stanley.[72] He finds this device more resistant to surface ionization and other radiation effects than any other active semiconductor device. However, surface ionization effects, especially on n-channel devices, produce large leakage currents across the gate-to-drain junction when the devices are operated under bias. This leakage current is important in the high-impedance circuits which use FETs.

Recent investigations have shown the metal-oxide-semiconductor field effect transistor (MOS-FET) to he quite sensitive to radiation due to surface effects. The MOS-FET is shown schematically in Fig. 30. The device consists of a base, in this case p-type Si, into which an n-type source and drain have been diffused. The conductivity of the base and hence the source-to-drain current, I_D, is controlled hy the potential applied to a metal gate electrode insulated from the semiconductor surface by a layer of SiO_2.

If a positive potential is applied to the gate, minority carriers are attracted to and majority carriers repelled from the base surface. As a result, an n-channel is formed between the source and drain. The conductivity of this channel depends on the gate potential, and thus the gate is able to control the drain current.

The effects of Co^{60} gamma radiation (simulating space environment conditions) on MOS-FETs have been studied by Hughes and Giroux[73,74] who found that the devices show changes in transconductance, g_m, and channel conductance at dose levels corresponding to short periods in space. Furthermore, the degradation appears to be hias-polarity dependent, as is evident in Fig. 31. Little or no effect is seen when the device is irradiated in the depletion mode, but large changes in the drain current and the transconductance are seen for irradiation in the enhancement mode. For n-channel devices, the zero gate voltage drain current ultimately increased from 1 mA to 45 mA in the enhancement

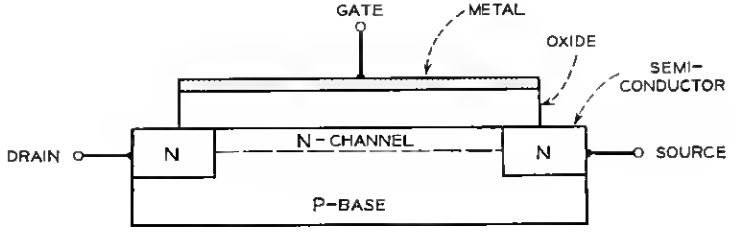

Fig. 30 — N-channel metal-oxide-semiconductor field effect transistor.

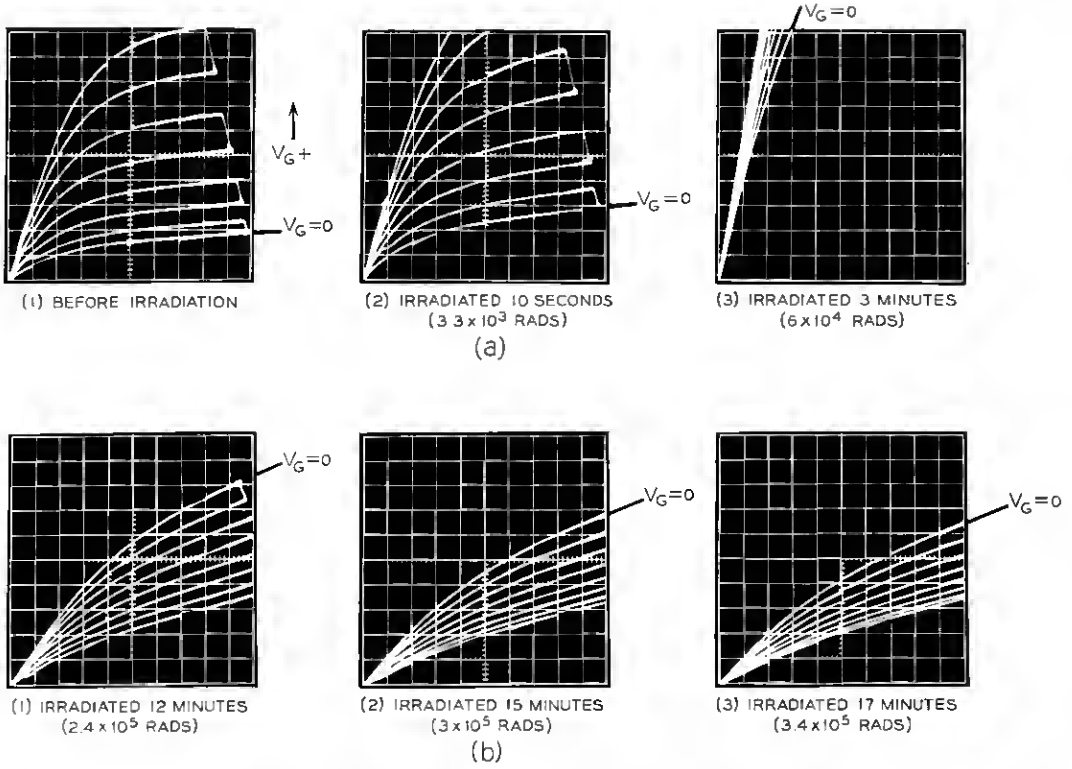

Fig. 31 — Effect of radiation on n-channel MOS-FET (after Hughes and Giroux, Ref. 74).

mode (gate biased positively with respect to the source) but showed little change in depletion mode (gate biased negatively with respect to the source) for a total dose of 10^6 rads. The effects of the radiation appear to he permanent with no apparent annealing after six months at room temperature.

The degradation of the MOS-FET ean be explained if it is assumed, as in the case of passivated transistors discussed earlier, that positive charges can be produced in the SiO_2 layer by radiation. In the enhancement mode, with the gate electrode positive, a strong electric field is set up which causes positive charge to migrate toward the Si–SiO_2 interface. Positive charge accumulation at this interface would, of course, increase the channel conductivity and drain eurrent. In the depletion mode, the field in the oxide will he reversed and positive charges will be attracted to the gate (where they have much less effect on the channel). Negative charge (in the form of electrons) migrating to the Si–SiO_2 interface will enter the Si and no negative charge will huild up at the interface.

To support this pieture, Hughes and Giroux ohserved the gate eapacities of n-channel MOS-FETs hiased in both the enhancement and depletion modes as a function of gate-to-source potential, V_{GS}, hefore and after 10^6 rads of Co^{60} gamma irradiation. The results are shown in Fig. 32. The capacitance minimum, which is observed as the gate voltage is increased from large negative values, occurs when the surface layer changes from depletion to inversion. If there were no charge stored at the Si–SiO_2 interface, the minimum should occur near $V_{GS} = 0$.

In the enhaneement mode, Fig. 32(a), the irradiation causes the minimum to shift -11.5 volts. This is to he expected if, as proposed above, a positive charge eollects at the Si–SiO_2 interface. For the depletion mode, Fig. 32(h), the minimum shifted only -1 volt indicating, as expected, rclatively little positive charge accumulation. From these results, Hughes and Giroux estimated that the capacity minimum shift for the enhancement mode corresponds to a positive charge layer of 10^{12} charges/cm^2 at the interface (this charge density would result from 10^{-3} monolayers of singly charged ions). The experiment was, however, incapable of giving information about the charge accumulation process or the nature of charge earriers.

The behavior of n-channel MOS devices in a radiation environment has been studied by Kooi using 150 keV X-rays.[54,75,76] The oxides used by Kooi were prepared in sevcral different ways and were all subjected to a P_2O_5 treatment. He found that irradiation caused a redistribution of charge within the oxide which depended strongly on the presence of electric fields. For positive values of gate potential Kooi observed a

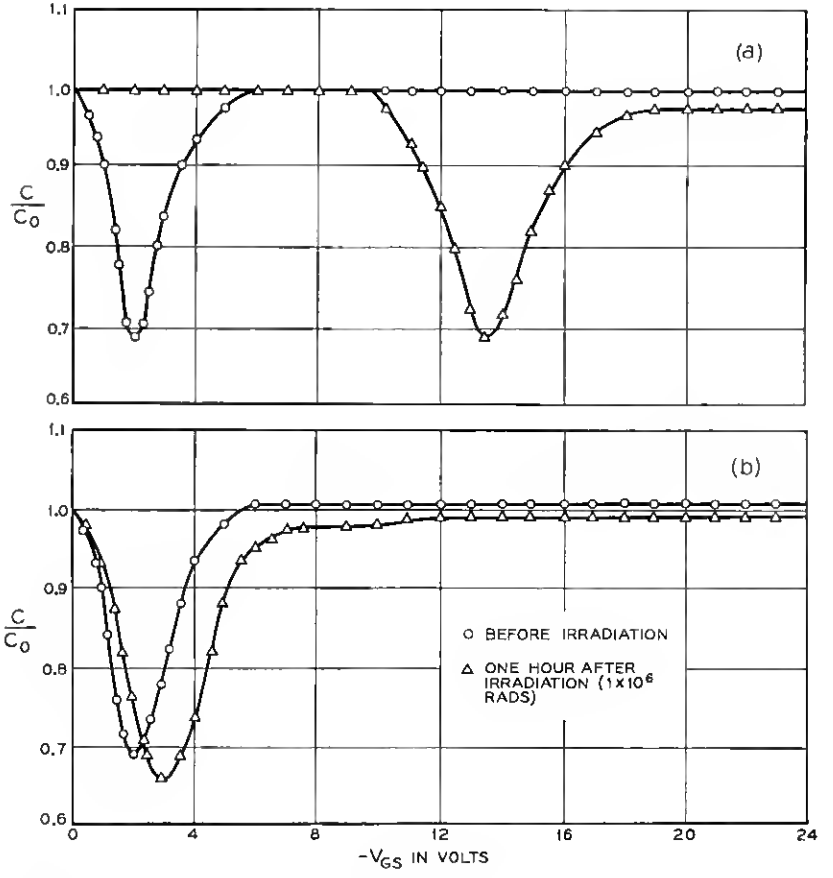

Fig. 32—Gate capacitance of an n-channel MOS-FET vs V_{GS} (after Hughes and Giroux, Ref. 74). (a) Enhancement mode, (b) depletion mode.

positive charge buildup in the oxide. The buildup was quite rapid and did not saturate. For negative gate potentials, on the other hand, a smaller positive charge buildup was observed which saturated after a few minutes exposure at 10^4 r/min. The saturation value was bias dependent.

Kooi explained his observations by supposing that the radiation caused the SiO_2 to become a photoconductor. For positive gate potentials electrons were removed from the oxide at the gate electrode. The Si was unable to supply electrons to the SiO_2 across the Si–SiO_2 interface. As a result a positive charge built up in the oxide. For a negative gate potential the electrons leave the SiO_2 and enter the Si. The metal-

oxide interface is now supposed hlocking and thus prevents electrons from entering the oxide. The result is again a positive charge buildup. In both cases the huildup will continue until the applied gate potential is entirely across the positive charge at which time the electric field elsewhere in the oxide will be zero. Thus, the buildup should reach a saturation value dependent ou the applied gate potential.

Kooi has also irradiated oxidized Si surfaces. Using MOS devices without gate electrodes be observed a positive charge buildup when the oxide was irradiated with 150 keV X-rays. However, when the oxide was subsequently exposed to ultraviolet light with photon energy $\geqq 4.2$ eV the positive charge was observed to decrease. Kooi explained the action of the ultraviolet light as follows: The ultraviolet light was only capable of exciting electrons onto the conduction hand in the Si hecause the energy gap of SiO_2 is several eV greater than 4.2. The excited electrons in the Si then enter the oxide and neutralize the trapped positive charge. A similar effect has been ohserved by Williams.[77]

Kooi also reported that the effects of radiation on SiO_2 depend strongly on the method of oxide preparation and on any subsequent heat treatment given the oxide. Furthermore, irradiation was able, in some cases, to alter the density of states at the Si–SiO_2 interface.

The degradation of enhancement mode, p-channel MOS-FETs irradiated with 1.5 MeV electrons has been studied by Stanley.[78] With a drain-to-source potential of -5 volts and the gate connected through 100 MΩ to the source, the drain current remained 5×10^{-10} A until the dose reached $5 \times 10^{+12}$ e/cm^2. At this dose, I_D increased rapidly and then saturated at $\approx 4 \times 10^{-5}$ A at $\approx 10^{14}$ e/cm^2.

The drain current as a function of the gate-to-source voltage, V_{GS}, is shown in Fig. 33 for three dose levels. Before irradiation, the turn-on voltage (i.e., the minimum value of V_G at which a channel is destroyed for a p-channel device or created for an n-channel device) is ≈ -3 volts. (This corresponds to the gate-source voltage where the drain current begins to increase rapidly.) After 10^{14} e/cm^2, however, the turn-on voltage has decreased to ≈ -10 volts and the current for positive V_{GS} values bas suhstantially increased. At 5×10^{14} e/cm^2 it is impossible to turn the device on.

The decrease in turn-on voltage can be explained in this case if it is again assumed that positive charge carriers are produced in the oxide hy radiation. The electric field in the oxide is in such a direction as to cause a positive charge buildup at the Si–SiO_2 interface. In this case, however, the positive charges cause an inversion layer (n-channel) on the p-type drain where it is overlapped hy the gate (see Fig. 34). A high density of positive charge must be present in the oxide, since it is difficult

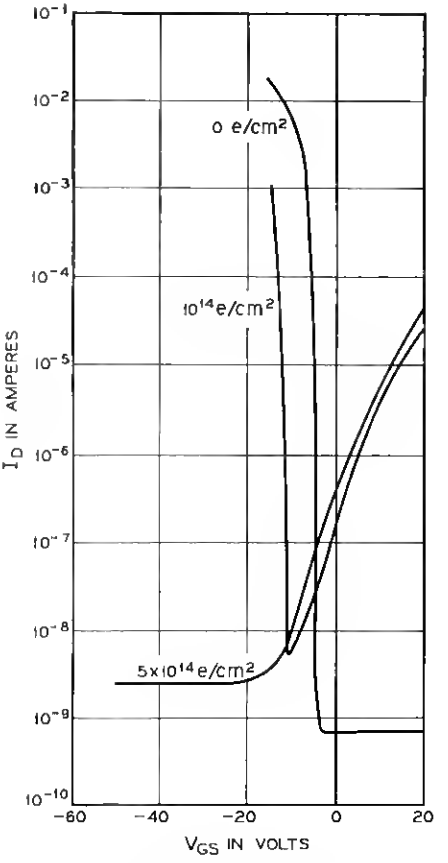

Fig. 33—Effects of electron irradiation on transfer characteristics; I_D vs V_{GS} at $V_{DS} = -20$V (after Stanley, Ref. 78).

to invert a highly-doped material such as the drain. As a result, the p-channel is isolated from the drain until the gate potential becomes negative enough to produce a p-channel deeper than the drain channel. With increasing radiation dose, the drain channel becomes deeper and the device more difficult to turn on.

The effect of low-energy electrons (10 to 20 keV) on the charge in au SiO_2 film on Si has been studied by Szedon and Sandor using an MOS capacitor.[79] As in the experiments of Hughes and Giroux, Szedon, and Sandor observed a shift in the C–V curve of the capacitor as a result of irradiation. From the results they estimated the density of surface states at the SiO_2–Si interface for two capacitors before and after radia-

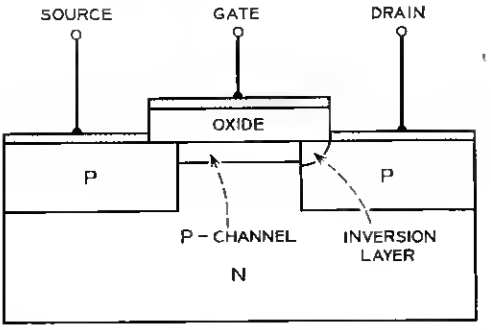

Fig. 34 — P-channel MOS-FET after irradiation (after Stanley, Ref. 78).

tion. The results are shown as a function of position in the energy gap of Si in Fig. 35. It can be seen for both capacitors that a significant number of states have been added, $\approx 2 \times 10^{12}$ states/cm^2—eV, over considerable portion of the energy gap. Szedon and Sandor also report that the effects of irradiation could be removed by a 15-minute anneal at 150-200 °C with the capacitor shorted.

Speth and Fang[80] have observed the changes in n-channel MOS-FET characteristics due to 5 keV electron bombardment. They irradiated the devices to a dose of $\approx 10^{14}$ e/cm^2 at successively larger positive values of gate voltage. At each gate potential value, V_G, the turn-on voltage of the device, V_T, stabilized at a more negative value indicating a buildup of positive charge in the oxide. The stable values of turn-on voltage were found to decrease linearly with increasing values of V_G used during irradiation. The effects of the radiation could be annealed out in several hours at 200 °C.

The effects of neutron irradiation on MOS transistors have been reported by Messenger and Steele.[81] They find the most important effect to be a positive charge buildup in the oxide, which causes the gate capacity minimum to move to more negative values of V_{GS}. They define the gate voltage at which the capacity minimum occurs as the turn-on voltage, V_T. Fig. 36 shows the change in V_T with neutron flux. According to Messenger, the tendency of V_T to saturate indicates a decreasing net accumulation rate of positive charge which may be caused by a diffusion or recombination process. The existence of such processes implies that the degradation should be dose-rate dependent and also the diffusion or recombination process has a substantially higher rate during irradiation since the degradation appears to be permanent after irradiation. At present there is no independent evidence to support this view. Annealing at elevated temperatures was found to

remove the degradation; typically, V_T showed 90 percent recovery after 70 hours at 150°C.

A study by Kuehne[82] of insulated gate thin-film transistors using polycrystalline CdS has revealed similar surface effects due to ionizing radiation. These devices showed bias-dependent semipermanent changes in transconductance and channel conductivity at doses of 10^5 rads. Analysis showed that interface trapping states are at least partly responsible.

5.7 *Integrated Circuits*

The direction of present-day semiconductor device technology is towards increased use of integrated circuits. These circuits contain many passivated areas where surface effects due to radiation may cause degradation. Unfortunately, very little work has yet been reported on surface effects of ionizing radiation on these devices. Stanley[83] has studied

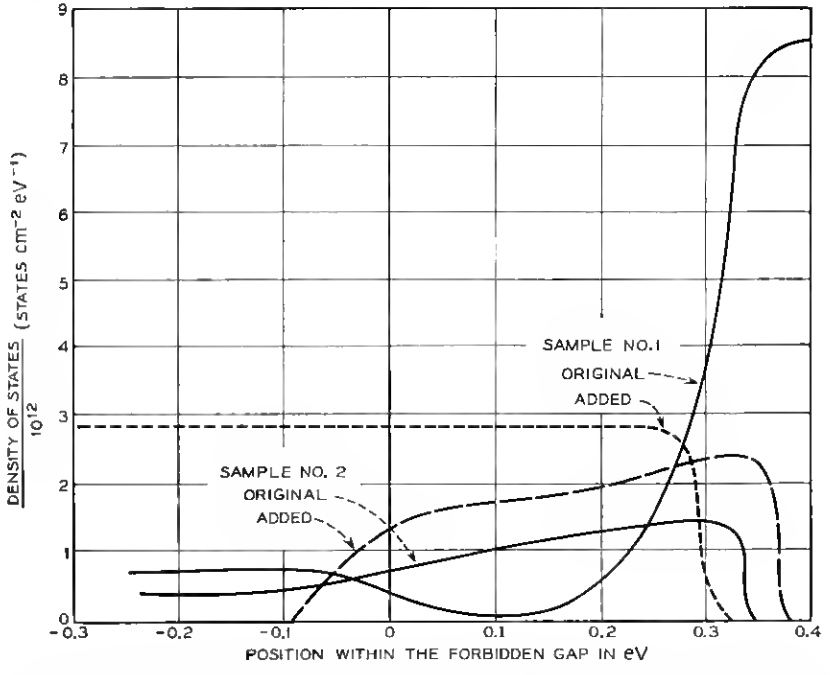

Fig. 35—Typical densities of states added by low energy electron bombardment of Al–SiO_2–Si capacitors, compared with original densities. Sample 1: 5Ω-cm n-type Si, 1600 Å oxide grown in wet O_2, capacitance-voltage data taken at 600 MHz. Sample 2: 50Ω-cm n-type Si, 1500 Å oxide grown in dry O_2; capacitance-voltage data taken at 1 MHz (after Szedon and Sandor, Ref. 79).

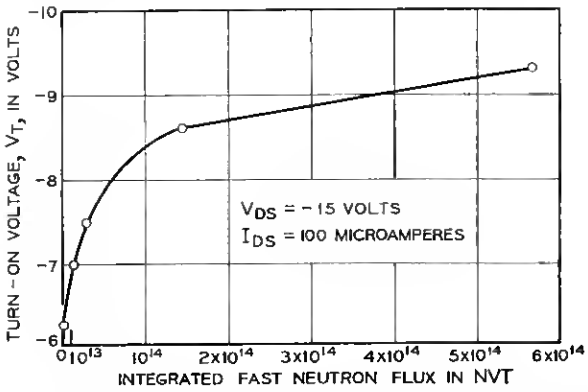

Fig. 36—Turn-on voltage vs neutron flux for a p-type MOS transistor (after Messenger and Steele, Ref. 81).

the effects of electron irradiation on a number of hybrid and monolithic integrated circuits. The hybrid circuits usually responded as would be expected from their component parts. Bulk and surface effects were difficult to separate in the monolithic circuits. It was apparent, however, that surface ionization did cause increases in I_{CEO} and decreases in h_{FE} for the integrated transistors.

VI. DISCUSSION

6.1 *Introduction*

The most recent trend in the electronics industry has been toward increasing use of silicon planar transistors, integrated circuits, and low-power devices such as the MOS-FET. Silicon dioxide films, in one way or another, are an integral part of these devices and it is necessary, therefore, that SiO_2 and its effect on devices be thoroughly understood. This is especially true in the case of radiation effects, since processes occurring in SiO_2 appear to be the cause of degradation. It is not surprising, then, that a large portion of this discussion is concerned with the problems of radiation effects in SiO_2 .

6.2 *Location of Surface Charge Responsible for Radiation Degradation of SiO_2-Protected Devices*

6.2.1 *Saturation Effects*

The results of the various studies on passivated bipolar and unipolar devices described earlier appear to be somewhat contradictory and

irreconcilable. The question is whether the surface charge which controls the degradation process is located on the outer surface of the oxide (Atalla's model[41]), or in the oxide at the Si–SiO_2 interface. It is not inconceivable, of course, that both views are valid and that under some circumstances charge on the SiO_2 surface dominates while in other cases charge within the oxide is more important. For some observations, both models are capable of an explanation. For example, Kerr,[61] Stanley,[64] Taulbee et al,[62] Brucker et al,[65,66] Speth and Fang[80] and to some extent Schmid[63] observe a saturation of degradation. Intuitively one would expect both models to predict saturation since both processes, surface charge separation and charge accumulation, are self-limiting.

6.2.2 *Importance of Bias*

With the exception of Schmid's observations, the experimental evidence indicates that bias is an important factor in degradation due to radiation. This result is not surprising since both models require an electric field; Atalla's model requires a parallel field component at the oxide surface, the other a transverse component in the oxide. These field components may arise from bias voltages across p-n junctions or from overlaying contacts.* It is also possible that built-in fields are produced in the SiO_2 layers during their formation. Built-in fields may reduce the dependence of degradation on bias voltage. At present it is difficult to predict quantitatively how degradation should depend on bias conditions and hence it is difficult to distinguish between the two models from the experimental results given above.

6.2.3 *Recovery of Surface Effects*

Recovery of passivated devices from surface effects due to radiation is to be expected under proper conditions for reasons similar to those for nonpassivated devices. Some recovery is expected to start as soon as the device is removed from the radiation. Removal of bias and increase in temperature should contribute to recovery; under these conditions, recovery has been observed as discussed above. One might, however, expect to see a difference in recovery depending on where the surface charge responsible for degradation is located. If the charge is located on the oxide surface, recovery might be somewhat easier than

* In most planar passivated transistors the evaporated emitter contact overlays the base region. Under reverse emitter bias, the field in the oxide may approach $\approx 10^5$ V per cm. In the case of an npn transistor, this field will tend to move positive charges in the oxide toward the oxide-semiconductor interface. For a pnp device, the positive charge will tend to move away from the interface. Base contacts do not generally overlay the collector and so comparable fields in the oxide at the base-collector interface do not occur.

it would be for a charge located inside the oxide, well isolated from the ambient. For example, simply exposing a nonpassivated device to the atmosphere can cause considerable recovery. For passivated devices, however, the bulk of the evidence points to a charge in the oxide, since recovery usually requires elevated temperatures; the degradation appears quite stable under shelf conditions, and exposure to the atmosphere does not produce noticeable recovery.

6.2.4 *Additional Evidence*

The model of charge storage in the oxide is further supported by Estrup's[84] finding that ion bombardment of passivated diodes did not produce the leakage current degradation observed with nonpassivated diodes. The strongest support, however, has come from the observation that degradation of irradiated passivated devices occurs even with a high vacuum ambient.[67]

All in all, the bulk of evidence supports the model of ionizable defects located in the oxide, apparently quite close to the SiO_2–Si interface, as being the principal source of degradation in these devices.

6.3 *Nature of the Charge in the Oxide*

Various defects and impurities, including sodium, aluminum, hydrogen, oxygen vacancies and trivalent silicon,[85] have been suggested, at one time or an other, as the species responsible for the positive charge buildup in SiO_2 layers. For SiO_2 layers subjected to elevated temperatures and electric fields, it appears that the accumulation of positive charge at the SiO_2–Si interface is the result of Na+ or H+ ion drift in the oxide. However, the questions of why a previously unstressed SiO_2 film should contain a positive charge and how radiation produces a charge buildup in the oxide are still not completely answered.

6.4 *Proposed Models of Charge Accumulation in SiO_2 Layers Exposed to Ionizing Radiation*

6.4.1 *Electron Drift Model*

Grove and Snow[86,87] have used MOS capacitance-voltage measurements to observe the buildup of positive charge in SiO_2 layers in MOS capacitors and transistors exposed to 35 keV X-rays. Witb negative values of gate voltage, V_G, (gate negative with respect to the silicon) they observed little change in the charge contained in the oxide. With positive values of V_G, on the other hand, appreciable buildup of positive charge was observed. For a given value of V_G, the charge density in

the oxide, Q_s, was observed to saturate with increasing radiation dose. The saturation value of charge density, Q_s (sat), was found to be proportional to $V_G^{\frac{1}{2}}$ for lower values of V_G.

Grove and Snow have proposed a quantitative model similar to the qualitative model suggested by Kooi,[75,76] which satisfactorily explains their findings. They assume the SiO_2 layer contains traps which are normally neutral. Upon irradiation the traps become positively ionized and the excited electrons drift to the positive gate under the action of the field in the oxide. The electrons are discharged at the gate. However, since the Si cannot supply electrons to the oxide, a positive space charge builds up at the SiO_2–Si interface.

The buildup of positive charge is best described with the aid of Fig. 37. Initially there is no charge in the oxide, Fig. 37(a), and consequently the field throughout the oxide is constant. As the positive charge accumulates in the oxide, Fig. 37(b), the charge on the gate decreases, the electric field in the oxide between the gate and space charge decreases, and the potential drop across the space charge region increases. After sufficient irradiation equilibrium will be achieved, Fig. 37(c), when the entire potential drop, V_G, appears across the space charge region. The electric field in the oxide between the gate and space charge will, of course, be zero. Further irradiation will not cause an increase in the space charge region unless V_G is increased.

To simplify calculations, Grove and Snow assumed that the density of traps, N_t, was constant throughout the oxide. Furthermore, they assumed all traps within a distance d of the SiO_2–Si interface were charged and that the traps elsewhere in the oxide were neutral. With these assumptions it can readily be shown that

$$d = (2K_0\epsilon_0 V_G/qN_t)^{\frac{1}{2}},$$

where K_0 is the dielectric constant of SiO_2, ϵ_0 is the permittivity of free space, and q is the charge on the electron. If V_G is reduced to zero, Q_s (sat) $(=qN_t d)$ will induce a negative charge, Q_s' (sat), in the silicon surface where

$$-Q_s'(\text{sat}) = qN_t d(1 - d/2x_0),$$

x_0 is the thickness of the oxide. (Q_s' (sat) is the quantity which is observed experimentally.) The observed values of Q_s' (sat) vs $V_G^{\frac{1}{2}}$ are shown in Fig. 38. Also plotted in this figure are three curves corresponding to the expression for Q_s' (sat) above with three different values of N_t assumed. Although the scatter of points is rather large, Q_s' (sat) appears to vary as $V_G^{\frac{1}{2}}$ for lower values of V_G as expected from the equa-

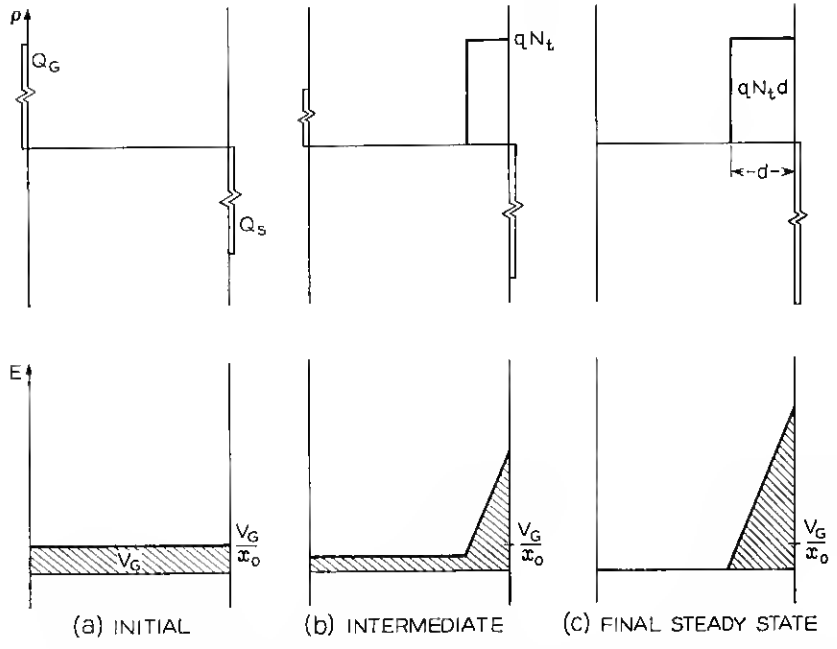

Fig. 37—Space charge buildup as a function of time during irradiation of a MOS structure under positive gate bias (after Grove and Snow, Ref. 87).

tion given above. The agreement with theory seems to be best for $N_t \approx 2 \times 10^{18}$ cm^{-3}.

Speth and Fang[80] have also employed a model which postulates a space charge buildup at the SiO_2–Si interface to explain their observations of the effects of low energy electrons (5 keV) on n-channel MOS-FET discussed previously, (Section 5.6). Using the calculations of Thomas and Young,[88] Speth and Fang predict that the turn-on voltage, V_T, of the MOS-FET should decrease linearly with increasing gate bias used during irradiation according to the equation

$$V_T = -V_G(2x_0/d - 1) + V_T^0 ,$$

where V_T^0 is the turn-on voltage prior to irradiation.

The basic difference between this model and the model of Grove and Snow is in the behavior of the space charge width, d. Speth and Fang assume d is independent of V_G. In other words, the space charge layer remains constant in width while the charge density within the space charge layer increases with irradiation. If, on the other hand, one follows Grove and Snow and allows d to increase while the charge density in the

space charge region is held fixed, d becomes a function of V_G as given above. The expression for V_T then becomes

$$V_T = V_G - (2qN_t x_0^2/K_0\epsilon_0)^{\frac{1}{2}} V_G^{\frac{1}{2}} + V_T^0 .$$

For reasonable values of N_t the second term on the right hand side of the equation dominates and $V_T \propto V_G^{\frac{1}{2}}$. Speth and Fang, however, observe a linear dependence of V_T on V_G in agreement with their expression for V_T. Snow[89] has suggested that the linear dependence observed by Speth and Fang may arise for quite a different reason. The 5 keV electrons used by Speth and Fang are not capable of penetrating the 1500 Å of Al gate and 6000 Å of SiO_2 insulation to reach the SiO_2–Si interface of the devices used. Instead, according to the range-energy relation of Katz and Penfold,[90] they are just able to penetrate the Al gate. Hence, the charge buildup should occur near the Al–SiO_2 rather than the SiO_2–Si interface. If one assumes a charge buildup as shown in Fig. 39, then it can be shown that

$$V_T = V_G + (qN_t x_0/K_0\epsilon_0)[x_1 - (x_1^2 + 2K_0\epsilon_0 V_G/qN_t)^{\frac{1}{2}}] + V_T^0 .$$

x_1 is the distance from the Si to the space charge region. If V_G is $\lesssim 5$ volts and $x_1 \gtrsim 700$ Å then it can be shown that

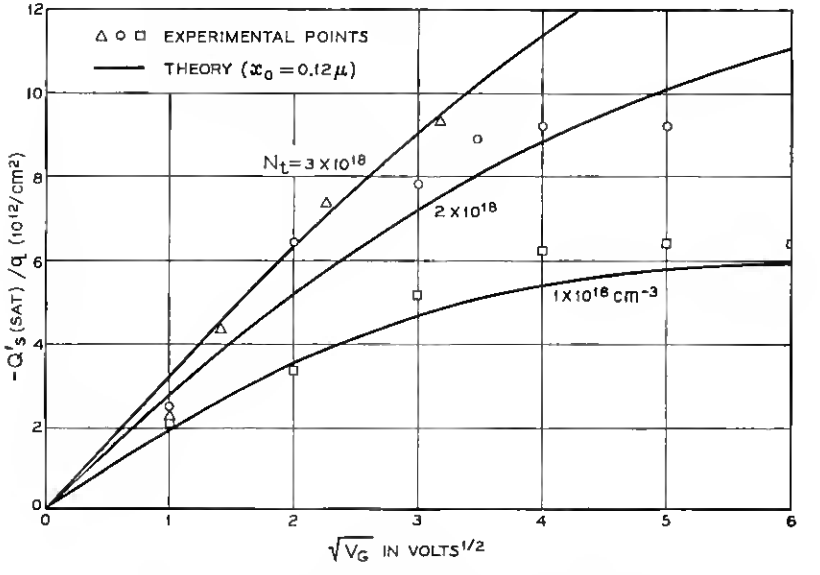

Fig. 38—Dependence of the saturation value of the excess charge induced in the silicon on the gate bias applied during irradiation. (after Grove and Snow, Ref. 86).

$$V_T \cong -V_G(x_0/x_1 - 1) + V_T^0 .$$

The approximate expression for V_T should apply to the results of Speth and Fang and V_T is expected to be linear with V_G. For the devices used, the slope of the graph of V_T vs V_G yields $x_0/x_1 - 1 = 13$ which, for $x_0 = 6000$ Å, gives $x_1 \cong 400$ Å. In other words, the positive charge accumulation in the SiO_2 may be far enough away from the Si–SiO_2 interface to make V_T appear linear with V_G.

The models employed by Grove and Snow and by Speth and Fang are, of course, oversimplifications of the true picture. The most obvious shortcomings are the neglect of the almost certain variation of N_t throughout the oxide and the assumption of an abrupt interface between the space charge and the neutral oxide. Nevertheless, such approximations are necessary in view of our very limited knowledge of the oxide.

The electron drift model requires further elaboration to explain what happens in the oxide when irradiation occurs with no applied electric field present in the oxide. The explanation may lie in the heterojunction picture of the SiO_2–Si interface proposed by Lindmayer and Busen.[91,92] According to this picture, SiO_2 is viewed as a wide gap insulator with a work function somewhat smaller than that of Si. When SiO_2 is grown on Si the work function difference, $\Delta\phi$, is accommodated by a transfer of electrons from the SiO_2 to the Si surface. These electrons come mainly from deep lying traps in the oxide. Hence, regardless of the conductivity type of the Si, the Si surface always tends to be n-type. The heterojunction picture thus offers an explanation of why the surface of freshly oxidized Si is invariably accumulated for n-type and depleted or inverted for p-type Si.

Initially the SiO_2–Si system may not be in equilibrium, i.e., insuf-

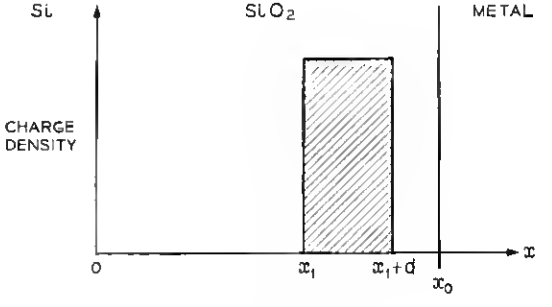

Fig. 39—Assumed charge distribution in the oxide.

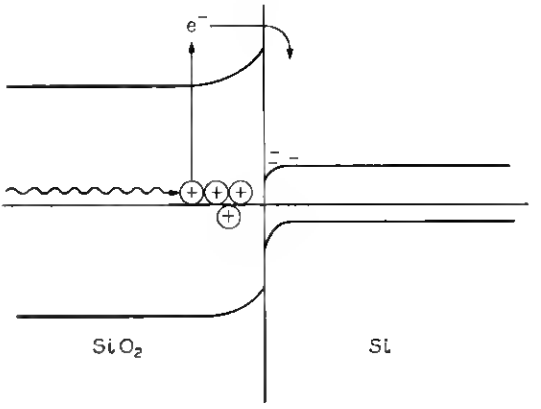

Fig. 40 — Transfer of electrons from SiO_2 to Si as a result of irradiation.

ficient positive charge may exist in the oxide after the growth of the film. Elevated temperatures or the presence of ionizing radiation may permit the system to equilibrate. Electrons excited into the conduction band of the oxide will diffuse to the interface and pass into the Si, see Fig. 40. Thus, positive charge may build up in the oxide even though no bias is applied to the gate. This buildup of positive charge will saturate, of course, when equilibrium is achieved. The positive charge density required for equilibrium for $\Delta\phi \approx 0.3$ eV is $10^{10} - 10^{11}$ charges cm^{-2}. Lindmayer and Busen report that annealing at 250°C for $\approx 10^3$ hours brought oxidized Si samples to equilibrium with positive charge densities in the oxide $\approx 10^{11}$ charges cm^{-2} even though the initial charge densities varied from 10^6 to 10^{11} charges cm^{-2}.

This particular heterojunction picture, is probably an over-simplification. A true heterojunction requires an abrupt interface between the two crystalline materials and the absence of a significant number of interface states.[93] For SiO_2 and Si, especially in the case of thermally grown oxide, the interface will not be abrupt; rather, there will be a transition region SiO_2–SiO_x–Si where x changes continuously from 0 to 2 on passing from the region of pure Si to the region of pure SiO_2. Furthermore, the charge storage effect should depend, quite noticeably, on the position of the Fermi level in the Si. Lindmayer and Busen, however, only discuss results on near intrinsic Si. Grove et al,[94] on the other hand, have examined oxidized p-type Si with a wide range of boron concentrations and report no appreciable variation of positive charge density.

6.4.2 *Positive Ion Drift Model*

As mentioned previously, positive ion drift is now widely believed to be the cause of charge buildup in SiO_2 layers exposed to elevated temperatures and positive gate bias. However, there is at present, little direct evidence that the effects of radiation on oxidized Si surfaces at room temperature are due to the migration of such ions. Nevertheless, it is interesting to speculate on a possible mechanism for radiation-induced charge buildup involving positive ions.

If one assumes that ionized (but not neutral) impurities are mobile in SiO_2 at sufficiently low temperatures then it is possible to construct a model for charge buildup. In this model the only requirement of the radiation is that it ionize a sufficient number of impurity atoms. The positively charged ions so produced would then drift through the oxide under the action of the applied field to the vicinity of the SiO_2–Si interface.

It is interesting to note that concentrations of Na^{50} and H^{47}, two possible charge carriers, are known to be highest near the metal-oxide interface. Thus, if the radiation has sufficient energy to penetrate the metal gate, it will be able to produce a large number of mobile positive ions. The ions will drift through the oxide and cause a buildup of charge at the SiO_2–Si interface. This model could, therefore, explain why the results of Speth and Fang indicate a charge buildup near the SiO_2–Si interface even though the radiation they used hardly penetrated to the oxide. Other results of electron irradiation on semiconductor devices indicate that degradation may occur at energies as low as 2.5 ± 0.5 keV[71].

At present the experiments of Grove and Snow support the view that charge buildup is primarily the result of ionization of existing traps rather than by the motion of ions. It may well be that both processes are possible and that the more important process in a given situation will depend on the energy of the radiation used.

6.5 *Recommendations for Future Surface Radiation Effects Studies*

6.5.1 *Fundamental Studies*

There is, at present, little information on radiation-indueed changes of the surface potential at a clean semiconductor surface. In principle, it would be relatively easy to study these changes by comparing the effects of radiation with those produced by, say, known ambient changes. In practice, reproducibly clean surfaces would be required and these are difficult to prepare and maintain. The radiation used should, of

course, be of low enough energy to prevent bulk damage effects (low-energy electrons might be suitable).

The effects of radiation-induced lattice damage at a semiconductor surface are unknown. Usually it is assumed that this type of damage is unimportant in a region such as a surface where lattice irregularities are already numerous. It is possible, however, that lattice damage sites may be created at energies significantly lower than in the bulk, and that these additional sites do, in fact, lead to an increase in the surface state density.

6.5.2 *Device Studies*

Continued emphasis should undoubtedly be placed on device studies, both for the role such studies play in validating the various models presented here and because the preparation of semiconductor surfaces by most of the device manufacturers has been a constantly evolving process. A short time ago a simple but satisfactory model of surface effects on (nonpassivated) devices existed. Today, however, the situation is, in a certain sense, worse since the problems of passivated devices are just beginning to be resolved.

Particular emphasis should be placed on understanding radiation surface effects in MOS-FETs, high-frequency transistors, thin-film transistors, metal-semiconductor junctions, and other low-level logic devices that are especially useful for low-power space applications. A model of the processes involved in the radiation-induced degradation of these devices should be developed. Ideally, such a model would of course, be most useful to device designers who could then design devices in such a way as to minimize the effects of radiation.

An important step in the development of a model would be the development of a surface stabilization technique which would reduce surface effects as much as possible. The charge transport mechanism in SiO_2 is now better understood and it may be possible to improve the passivation process to provide even better and more stable surfaces. Perhaps the P_2O_5 treatment of SiO_2 or the use of other passivation materials such as silicon nitride will provide the improved stability.

At present, the method of oxide preparation varies from manufacturer to manufacturer, making it difficult to interpret results from different sources. It may prove necessary to develop a standard procedure for device passivation, at least for devices exposed to radiation. Other manufacturing steps, such as the deposition of contacts or the bonding of leads, may lead to local damage areas. These areas may be more sensitive to radiation effects and should be investigated.

It is essential that the effects of ionizing radiation on metal-semiconductor and heterojunction interfaces be understood. This important area has heretofore been neglected. Studies of noise arising from surface effects in both unipolar and bipolar devices is another area that has unfortunately been neglected. Noise in MOS structures has been discussed by Sah[95] and by Jordan and Jordan,[96] but a study of the effects of radiation on noise in MOS devices has not been reported.

6.5.3 *Procedures for Selecting Devices for a Radiation Environment*

Ultimately, the device studies outlined above should lead to procedures for selecting both the type and individual device best suited with respect to surface effects for use in a radiation environment. To date, very little has been done to evolve such procedures. Peck et al,[23] in choosing transistors for the *Telstar*® satellite, devised a straightforward selection process. The various device types were subjected to a gamma exposure of 1.4×10^4 rads (8.5×10^5 rads/hr for 1 min) followed by an exposure at 3 rads/hr for at least one week. Device types showing no significant changes in I_{CBO} and h_{FE} were considered satisfactory.

Peck et al also studied screening and selection procedures using diffused Si transistors. They showed that, by selecting devices which had an I_{CBO} value of less than 10^{-8} A after a screening dose of $\approx 10^4$ rads, they could eliminate 90 percent of the devices which ultimately suffered severe I_{CBO} or h_{FE} degradation.

A selection procedure for planar Si transistors which uses microplasma noise measurements in addition to a screening radiation procedure has been developed by Bostian and Manning.[97] According to these investigators, microplasma noise is an indicator of the presence of surface defects which act as acceptor states. These acceptor states aid in channel formation on pnp devices and oppose it on npn. Thus pnp transistors exhibiting the least microplasma noise and npn exhibiting the highest should be least susceptible to radiation.

Based on the above model, Bostian and Manning give a selection procedure. First, select transistor types with the highest upper frequency limit to reduce gain degradation due to bulk radiation damage. Next, select the pnp transistor type with the lowest or the npn type with the highest average microplasma noise level. Then, select the individual devices by choosing the pnp's with lowest and the npn's with the highest noise levels. Finally, expose the devices to a screening dose of 5×10^4 rads and reject any showing I_{CBO} values significantly above average.

Using the procedure outlined above, the authors report improvement

factors (defined as the ratio of average leakage current of all devices in a group to the average current for selected devices) of about 10, depending on device type.

VII. SUMMARY

The degradation of many semiconductor devices resulting from surface effects of radiation may be explained, qualitatively at least, using the presently accepted model of semiconductor surfaces. The explanations are based on the creation by ionizing radiation of localized charged energy states on semiconductor surfaces.

These states are created both at the termination of a semiconductor lattice itself, the so-called "fast" states, and in any surface layer, such as an oxide, the so-called "slow" states. The slow states are usually the more numerous and the charge they contain controls the surface potential and hence the number and type of charge carriers in the surface region. The fast states, on the other hand, are the states which actually interact directly with the charge carriers in the semiconductor. They act as generation and recombination centers for holes and electrons, and their activity is measured by the surface recombination velocity, which depends on the surface potential.

As a result of irradiation, a device accumulates charge principally in the slow states, and this charge affects the underlying semiconductor surface. As a result of changes in the surface potential, the surface recombination-generation may be increased (because of changes in both the surface recombination velocity and the number of fast states), causing device degradation. Inversion layers (channels) may also be formed at p-n junctions, leading to increased reverse leakage currents and degraded emitter efficiency.

For nonpassivated devices, the slow states are in close proximity to the surface and hence strongly influence the surface layer. These devices are, therefore, very sensitive to ambient changes such as those caused by radiation. In passivated devices, the slow states tend to be further removed from the semiconductor surface, and hence these devices are generally one or two orders of magnitude less sensitive to radiation.

For nonpassivated devices in a gaseous ambient, the mechanism by which radiation produces charge in the slow surface states is reasonably well established. Radiation produces gaseous ions, some of which are attracted by electric fields to the device surface, where they subsequently deposit charge. When sufficient ionic charge (generally positive) has been collected on the surface, inversion layers (channels) form on the underlying semiconductor which in turn alter junction

leakage currents and transistor gain. For a pnp device, channels tend to form on the p-type collector side, causing large increases in I_{CBO}. The surface recombination in the emitter-base region is relatively unaffected by this positive surface charge, and therefore the h_{FE} degradation is usually small. For npn transistors, on the other hand, the channel forms on the base. Because the base width of a transistor is usually small, this channel is restricted in size and hence I_{CBO} does not generally increase as much as for pnp devices. However, generation-recombination current at the emitter-base surface is increased, causing a large decrease in h_{FE}. If the base channel extends from the collector to the emitter, then I_{CEO} will increase and h_{FE} may appear to increase because of the increase in I_C.

The simple model used to explain the degradation of nonpassivated devices is of somewhat limited usefulness. It does predict the bias dependence of degradation and also the recovery of devices under proper conditions. However, this model at present does not explain the observed memory effects, nor does it generally apply to devices with grease or similar ambients.

The number of passivated Si planar devices has greatly increased in the past few years and will most likely continue to do so in the future. Thermally grown SiO_2 films are used to passivate the surfaces of these devices by stabilizing the interface structure and isolating the Si from the ambient. The SiO_2 film becomes, therefore, an integral part of the device and it is necessary to understand the role this passivation layer plays when the device is subjected to radiation.

It is well established that passivated devices degrade in ways quite similar to nonpassivated devices when exposed to radiation, although they are generally less sensitive than their nonpassivated counterparts. The degradation appears to result from the formation of positive surface charge in or on the oxide, with the consequent production of channels on the device surface. The channels manifest themselves by increased junction leakage currents and reduced transistor gain. The behavior of npn and pnp transistors follows the pattern outlined above for the nonpassivated case. Passivated devices also exhibit memory and recovery effects similar to those observed with nonpassivated devices.

The main point of controversy among the models used to explain the degradation is the process by which the positive surface charge accumulates. In one view, the charge is created by ionization of impurities on the surface of the oxide, and these ions are then separated by surface electric fields. The majority of experiments, however, indicate

that the charge exists within the SiO_2 , prohahly close to the SiO_2–Si interface. Several species of charge carrier, including Na^+ and H^+ ions and electrons, have heen suggested as the means by which charge is transported through the oxide. None of these has, as yet, heen conclusively demonstrated as the responsible carrier, nor has the role played by radiation in the accumulation process been clarified.

MOS-FETs have been shown to be quite sensitive to radiation, more sensitive than conventional passivated devices. The cause again appears to he positive charge accumulation in the oxide near the SiO_2–Si interface. Presumahly, the explanations of degradation in MOS-FETs and passivated devices will he very similar, since the same oxide is used in hoth cases.

It has heen found experimentally that oxide-covered Si surfaces invariably tend to he n-type regardless of the conductivity type of the Si. This fact implies the existence of a rather large built-in positive charge in the oxide after the growth of the film. If the SiO_2–Si interface is viewed as a heterojunction, it can be shown that, as a natural result of the work function difference hetween the SiO_2 and the Si, the Si surface should have an equilihrium charge density of $\approx 10^{11}$ electrons-cm^{-2}. The oxide will, of course, have a positive charge density of equal magnitude.

It may well he that, during growth of an SiO_2 film, the equilihrium charge density is uot attained. Furthermore, it cannot he attained after growth at room temperature since the oxide cannot supply sufficient electrons to the Si hecause of the large energy gap of the oxide. Radiation will, however, cause ionization in the SiO_2 and allow at least some equilihration of charge, i.e., further accumulation of positive charge in the oxide.

A model has been suggested hy Kooi and elahorated by Grove and Snow for an oxide irradiated in the presence of an applied electric field in which electrons excited out of traps drift out of the oxide into the gate for positive and into the Si for negative gate potentials. For positive gate hias the electrons which leave the oxide are not replaced since the Si cannot supply electrons to the oxide. A positive charge huildup at the SiO_2–Si interface results. For a negative gate bias, on the other hand, the gate replaces electrons which leave the oxide and enter the Si. Hence, there is no charge huildup. An alternative model for which there is as yet little evidence assumes that positive ions may be sufficiently mohile at low temperatures ($\lesssim 100°C$) to drift under the action of applied electric fields and huild up a positive charge at the SiO_2–Si interface.

The need for further work on both fundamental and practical problems in surface radiation effects is self-evident. Devices, particularly those suitable for low-level logic in space applications, will require extensive study, since these device types are likely to be quite sensitive to surface radiation effects.

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APPENDIX A

Units of Radiation Commonly Used in Surface Effects Studies

There are two units of radiation in common use in surface effects studies. The roentgen (r) is a unit of radiation exposed dose and is defined as that quantity of X- or gamma-radiation which produces 2.083×10^9 ion pairs per cc of air at standard conditions. The amount of radiation absorbed from a given exposed dose, however, will depend on the absorbing material. An irradiated material is said to have received an absorbed dose of one rad when it has absorbed 100 ergs per gram of irradiated material. Calculation of an absorbed dose requires a knowledge of the energy of the radiation and the appropriate absorption coefficients of the material. For Si devices exposed to Co^{60} gamma radiation it is usually assumed that an exposure dose of 1 roentgen results in an absorbed dose of $\approx$1 rad.

APPENDIX B

Calculation of Absorbed Dose from Electron Irradiation

The purpose of this appendix is to illustrate a method of calculating the radiation absorbed dose (in rads, say) for an SiO_2-protected Si planar device exposed to a beam of mono-energetic electrons. To simplify the calculations we will consider that device degradation (due to surface effects) occurs only as the result of ionization produced in the SiO_2 layer and that ionization produced anywhere in the oxide is equally effective. In other words, only the total energy absorbed by the oxide is important.

For the purposes of calculating the absorbed dose, one of three possible situations will occur depending on the energy of the electrons and the thickness of the oxide. The three cases are:

(*i*) The electrons are completely stopped in the oxide.

(*ii*) The electrons penetrate the oxide and lose a significant fraction of their energy in so doing, i.e., the oxide thickness is comparable to but less than the range of the electrons.

(*iii*) The electrons penetrate the oxide without a significant loss of energy, i.e., the oxide thickness $\ll$ the range of the electrons.

To decide which of the three cases is applicable it is necessary to know the range, R, of electrons in SiO_2 as a function of electron energy, E. Fig. 41 shows this relationship according to the range-energy equation of Katz and Penfold.[90] A density of 2.66 gm/cm^3 has been assumed for SiO_2 . The curve has been extrapolated to an energy of 10^{-3} MeV although Katz and Penfold give 10^{-2} MeV as the lower limit of accuracy for their equation.

For the sake of a concrete example, let us assume that we wish to know the absorbed dose as a function of electron energy for a 1μ thick oxide layer on a semi-infinite Si substrate when a beam of 1 electron/cm^2 is incident normally on the oxide (see insert in Fig. 43). From Fig. 41 it is apparent that electrons with energies $\leqq 1.3 \times 10^{-2}$ MeV will be completely stopped by the oxide, case (*i*) above. For this case it is assumed that all the energy of the electrons is absorbed by the oxide and hence the calculation of the absorbed dose is quite straightforward.

For electron energies $\geqq 4.2 \times 10^{-2}$ MeV the range of the electrons is $\geqq 10\mu$ compared to the 1μ thickness of the oxide and therefore the electrons will lose only a small fraction of their energy in passing through the oxide, case (*iii*) above. For this case we need to know the stopping power, $(-dE/dx)$, of the oxide as a function of electron energy. According to Bethe[98], the stopping power for electrons of energy E is given by,

$$-dE/dx = \frac{2\pi e^4}{mv^2} N_e[\ln mv^2E/2I^2(1-\beta^2) - (2\sqrt{1-\beta^2} - 1 + \beta^2)\ln 2 + 1 - \beta^2 + \tfrac{1}{8}(1-\sqrt{1-\beta^2})^2 - \delta] \text{ ergs/cm},$$

where

e = electronic charge in esu
m = electron rest mass in grams

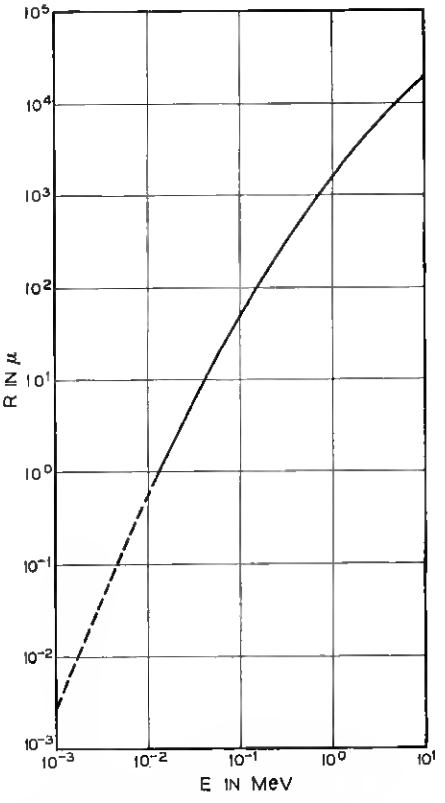

Fig. 41 — Range-energy relationship for electrons in SiO_2.

v = electron velocity in cm/s
N_e = density of electrons in stopping material
I = mean excitation potential of stopping material
β = v/c
c = velocity of light in cm/s
δ = correction for density effect.

The stopping power for electrons in SiO_2, as calculated from the above expression, is shown in Fig. 42. N_e for SiO_2 was estimated to be $7.9_6 \times 10^{23}$ e/cm^3 and a value of 1.2×10^2 eV was assumed for I. The density effect correction term, δ, was taken as zero for the solid curve. However, δ becomes important for $E \geqq 0.5$ MeV and can amount to $\approx$10 − 15 percent at 10 MeV. The dashed curve indicates the effect of this correction.

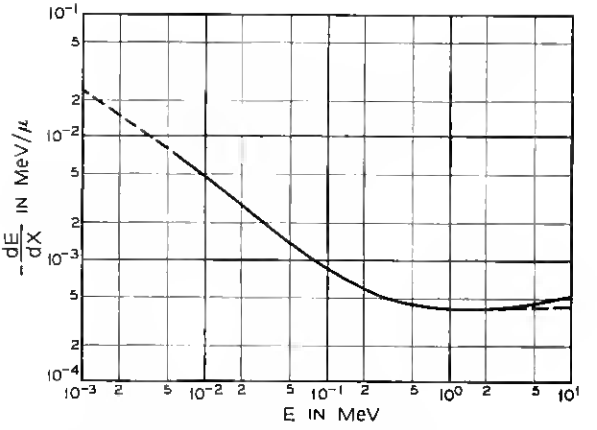

Fig. 42—Stopping power of SiO_2 for electrons as a function of electron energy.

For the case under consideration we will assume the absorbed dose at high energies ($\geqq 4.2 \times 10^{-2}$ MeV) will be equal to the product of the stopping power and the oxide thickness. This assumption is not altogether justified, however, since at higher energies a significant portion of the energy lost by the electron in traversing the oxide will appear as bremsstrahlung and will, therefore, not be absorbed by the oxide. At 10 MeV $\approx$15 percent of the energy lost by the electron in the oxide will appear as radiation.

The absorbed dose in the 1μ of oxide due to an exposed dose of 1 electron/cm^2 is shown in Fig. 43. The curve is divided into three regions corresponding to the three cases discussed above. Case (*ii*), which is difficult to analyze quantitatively, has been interpolated between the other two cases. The effect of loss due to radiation in case (*iii*) has been indicated by the dashed curve.

It is apparent that the maximum absorbed dose, for a given incident particle flux, is obtained with electrons whose range is just equal to the oxide thickness. It is interesting to note that for high energy electrons ($\geqq$1 MeV for a 1μ thick oxide) the absorbed dose is more than an order of magnitude smaller than the maximum. It has been customary to report an exposed dose for electron irradiation in terms of electron energy and integrated particle flux. In the energy range 0.5 to 5.0 MeV the absorbed dose per electron is roughly constant ($\approx 3 \times 10^{-8}$ rads/e-cm^{-2}). However, outside this range there is considerable variation of absorbed dose with electron energy, and it would appear necessary to convert from exposed to absorbed dose, as outlined above, if a comparison

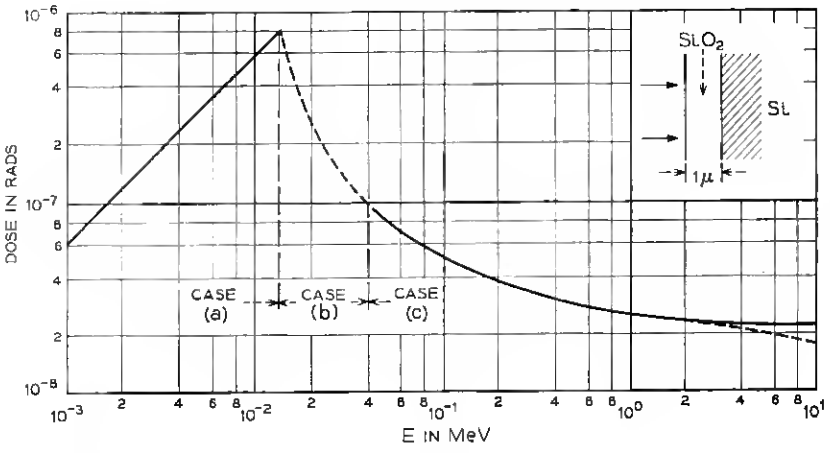

Fig. 43 — Absorbed dose per e/cm² for a 1μ thick SiO_2 layer as a function of electron energy.

among results reported at different energies is to be made. If a metal layer is present on the surface of the oxide it will be necessary to make an appropriate correction. This correction will be most important for cases (*i*) and (*ii*) above.

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